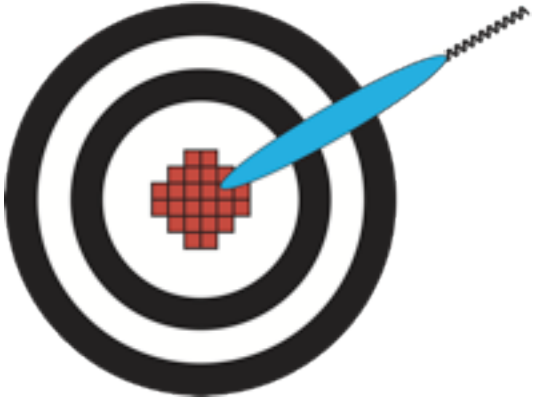
Cherenkov Telescope Array readout electronics



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Stefan Funk, Sonia Karkar, Akira Okumura, Leonid Sapozhnikov,
Hiro Tajima, Luigi Tibaldo, Gary Varner

Imaging the Extreme Universe: Solid-state Cameras for Astroparticle Physics
Kavli Institute for Cosmological Physics, University of Chicago
May 10, 2013

Outline

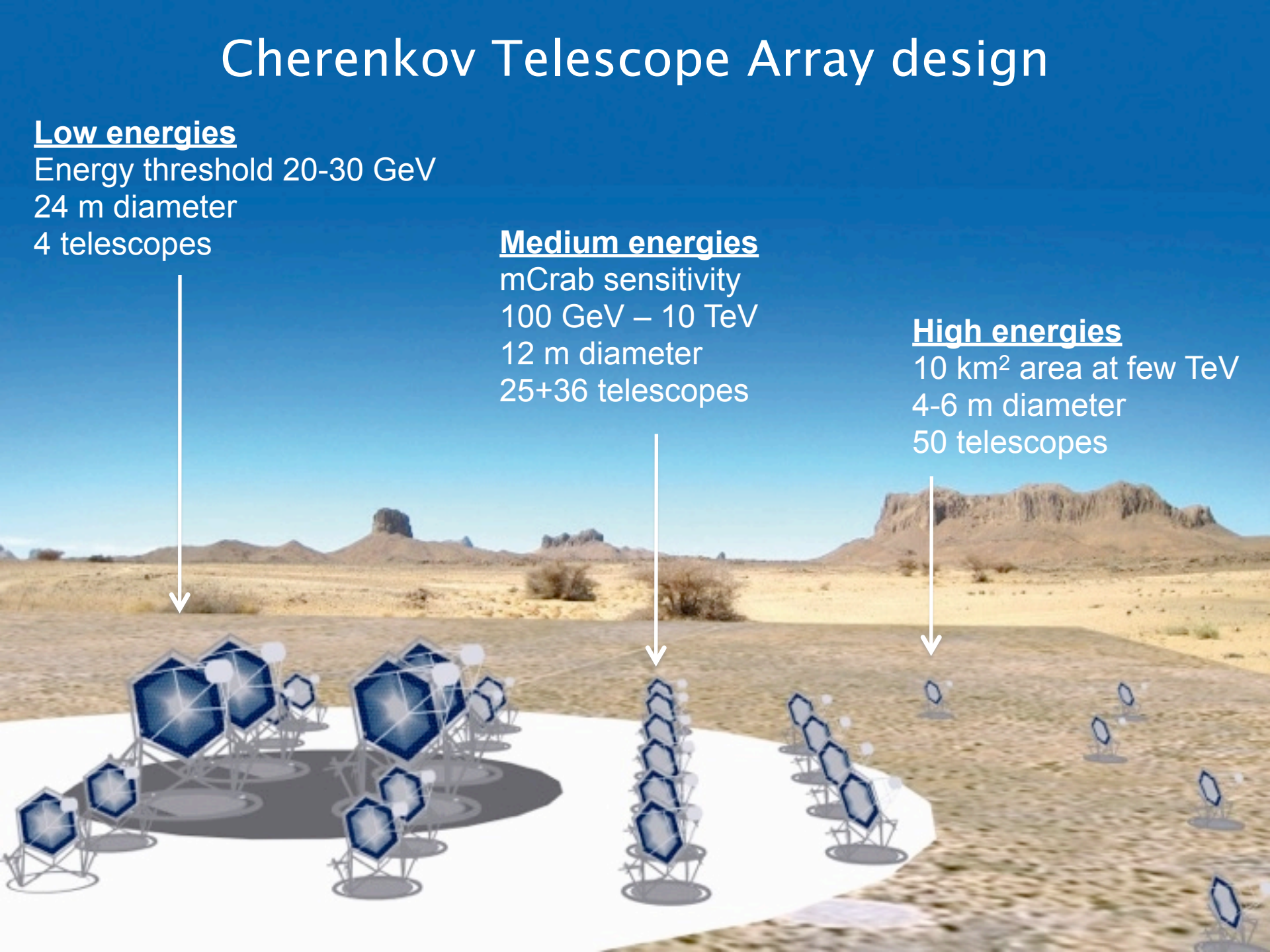
- Dual-mirror telescopes in CTA
- Modular camera design
- Analog sampling
- Trigger
- Digitization

Cherenkov Telescope Array design

Low energies
Energy threshold 20-30 GeV
24 m diameter
4 telescopes

Medium energies
mCrab sensitivity
100 GeV – 10 TeV
12 m diameter
25+36 telescopes

High energies
10 km^2 area at few TeV
4-6 m diameter
50 telescopes

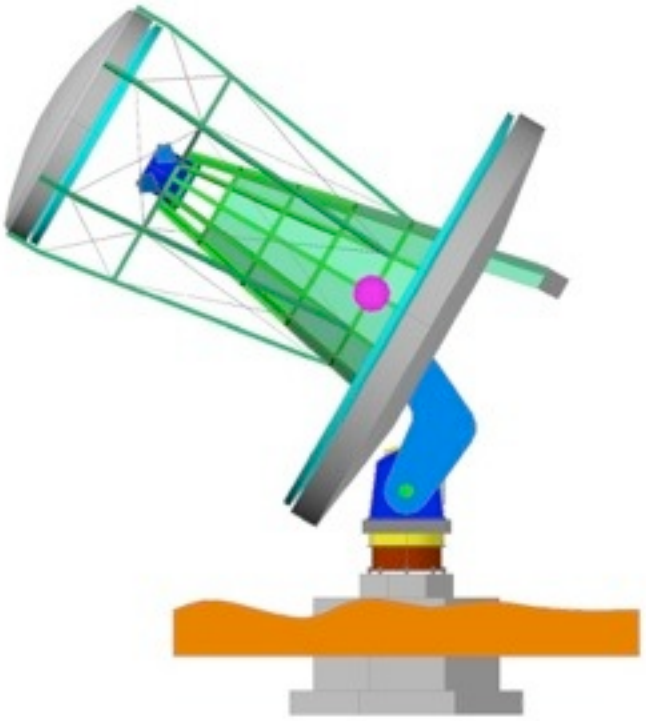


TARGET in CTA

- TARGET chips will be deployed in 3 prototype CTA cameras
- US-led Schwarzschild-Couder (two-mirror) mid-size telescope (for core energy range), using silicon photomultipliers
- UK-led camera for highest energy gamma-rays ("Compact High-Energy Camera")
  - One using multi-anode PMTs
  - One using silicon photomultipliers

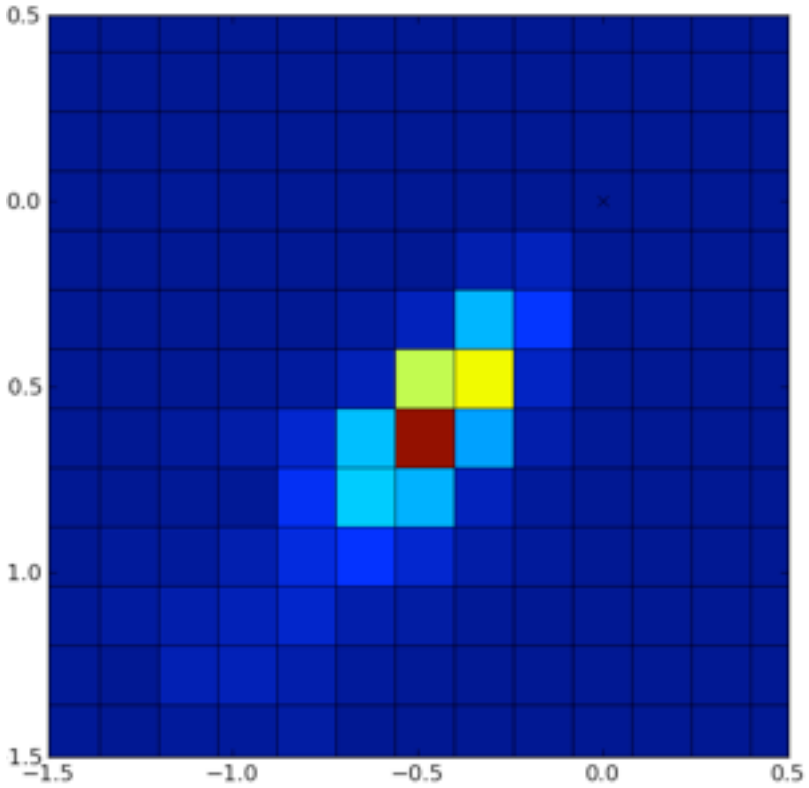
US focus: mid-size dual-mirror (Schwarzschild-Couder) telescopes

- Allows better optical PSF over wide (8° diameter) field of view and small camera focal plane
- Small focal plane well suited for modern dense, highly integrated photo-detectors (MAPMTs and SiPMs) and electronics (application-specific integrated circuits)
- Improved gamma-ray angular resolution and background rejection allow qualitatively improved sensitivity
- R&D and prototyping underway on dual-mirror design
- Current design: 9 m primary diameter

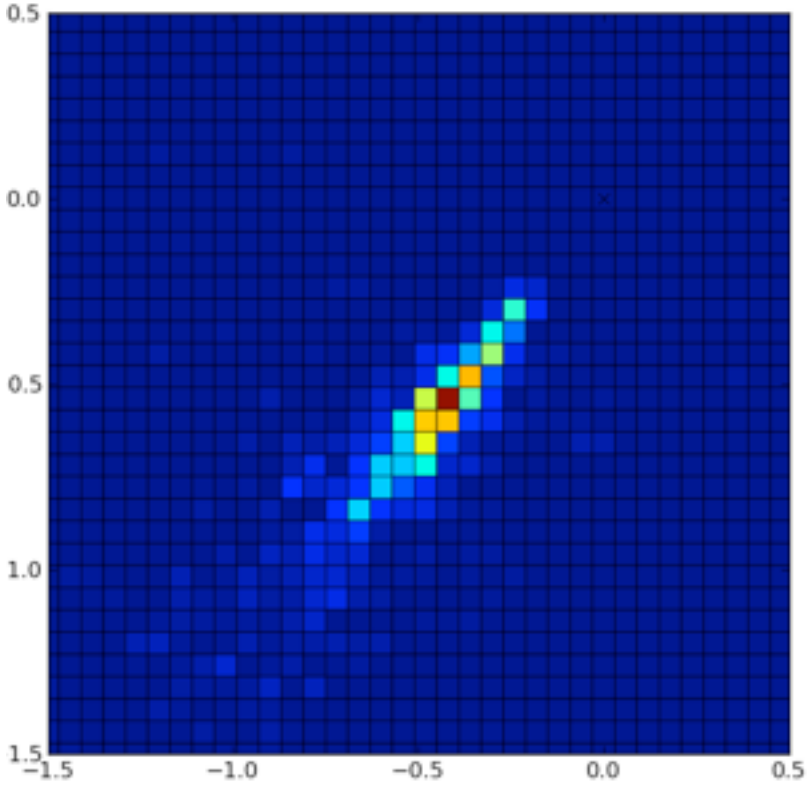


Simulated shower images for DC vs. SC telescopes

Example 1 TeV gamma-ray shower as seen by one-mirror or two-mirror telescope



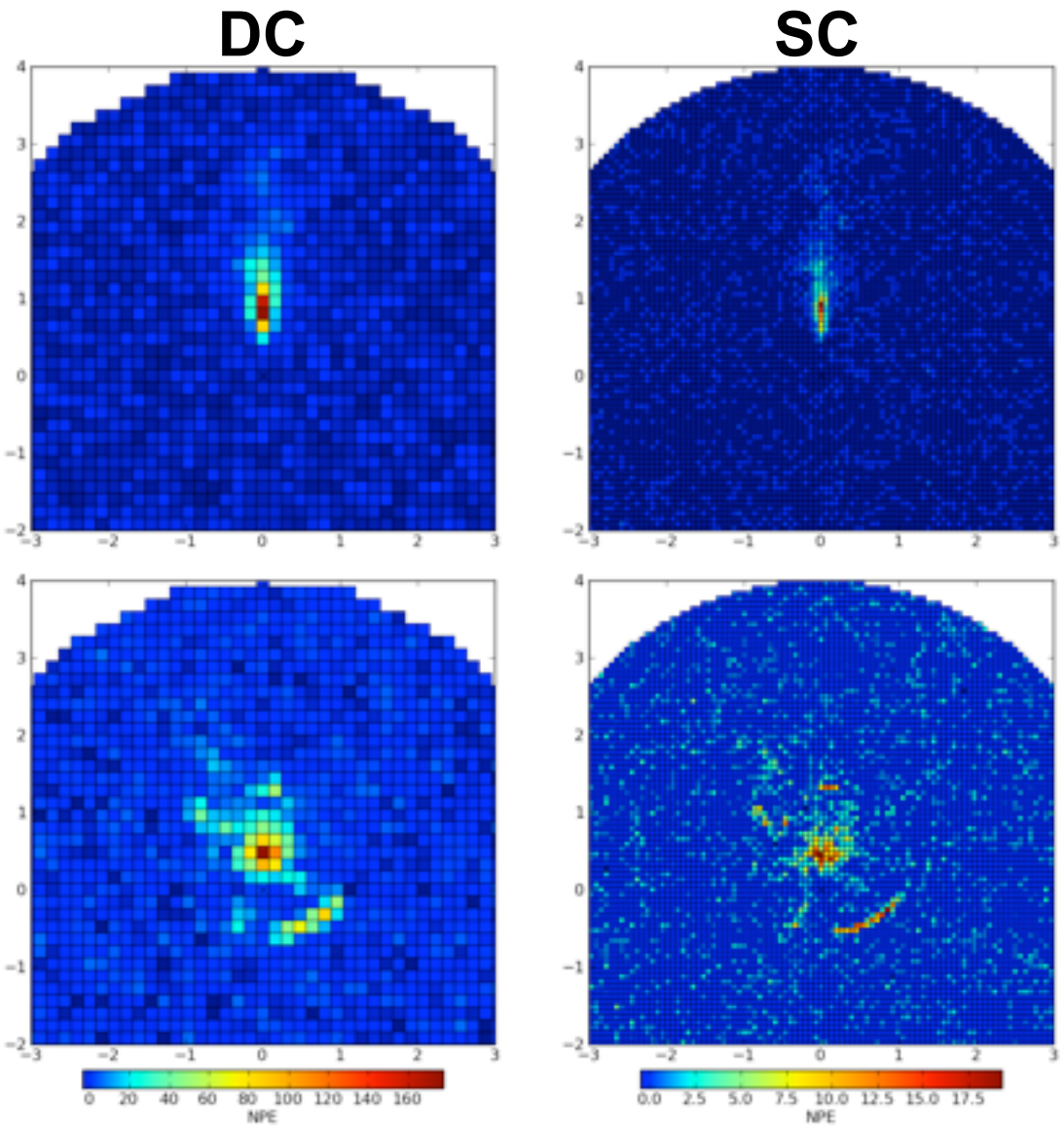
DC telescope (~2k 0.16° pixels)



SC telescope (~10k 0.06° pixels)

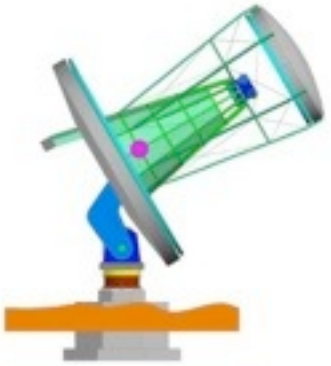
Both images zoomed in (2° across, compared to 8° field of view)

DC vs. SC images for signal and background



NSF-funded prototype project

- Prototype project funded by NSF Major Research Instrumentation (MRI) program
- Fall 2012 – Fall 2015
- Constructing the first Schwarzschild-Couder telescope
- At VERITAS site in Arizona
- At end of MRI project, will submit full NSF/DOE proposal for US CTA contribution of up to 36 two-mirror or single-mirror telescopes

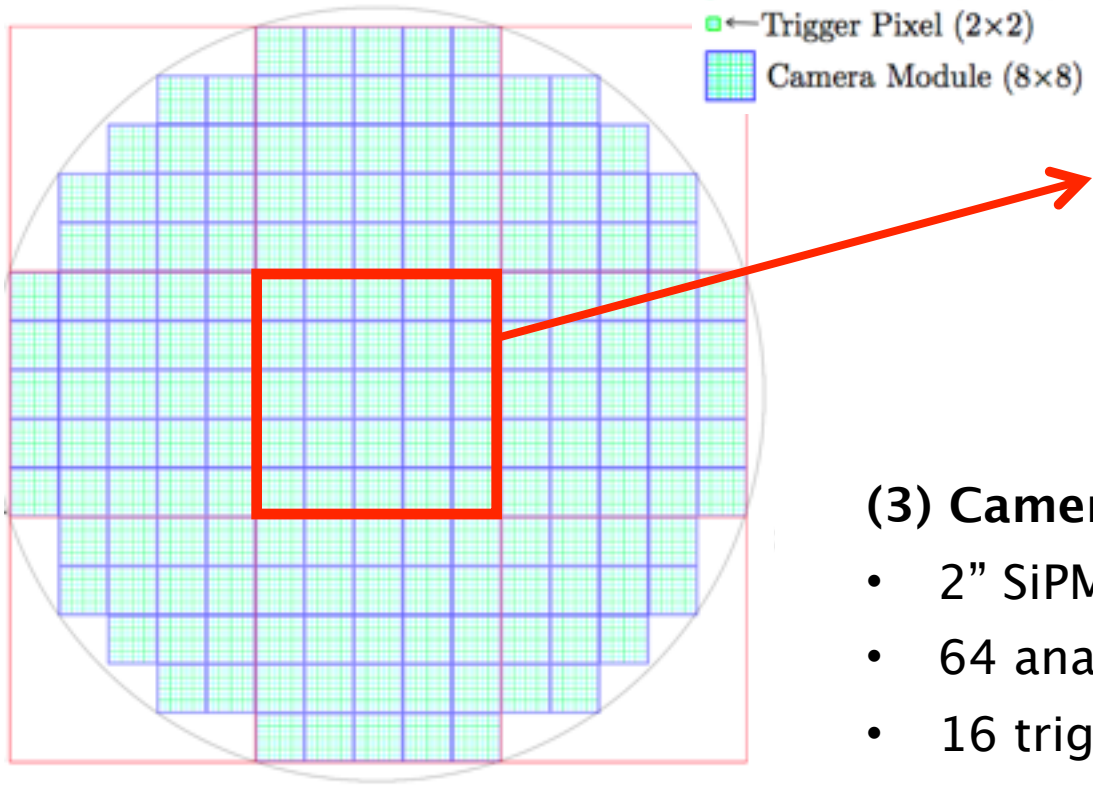


VERITAS site

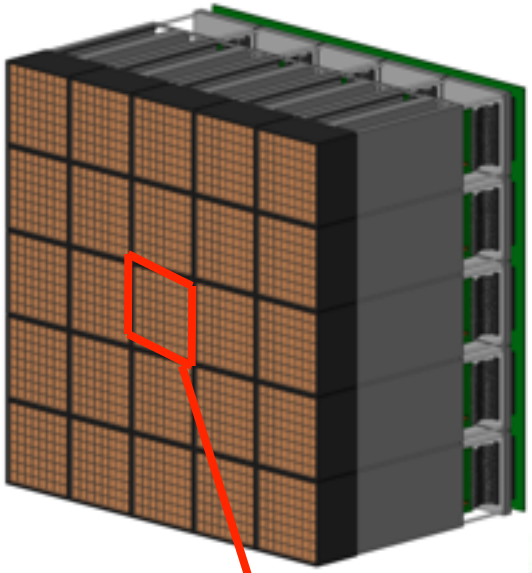
Modular camera design for Mid Size Telescopes

(1) Full camera: 9 sub-fields

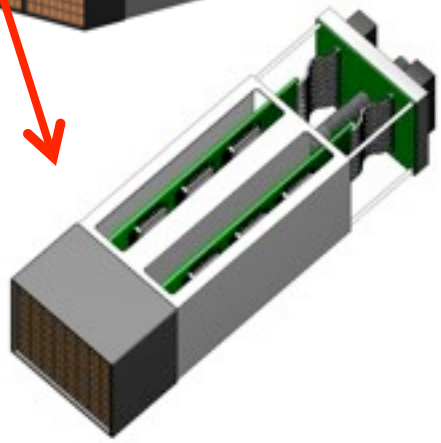
8° (0.8 m) diameter for 11,328 pixels (177 modules)



(2) Sub-field: 25 modules



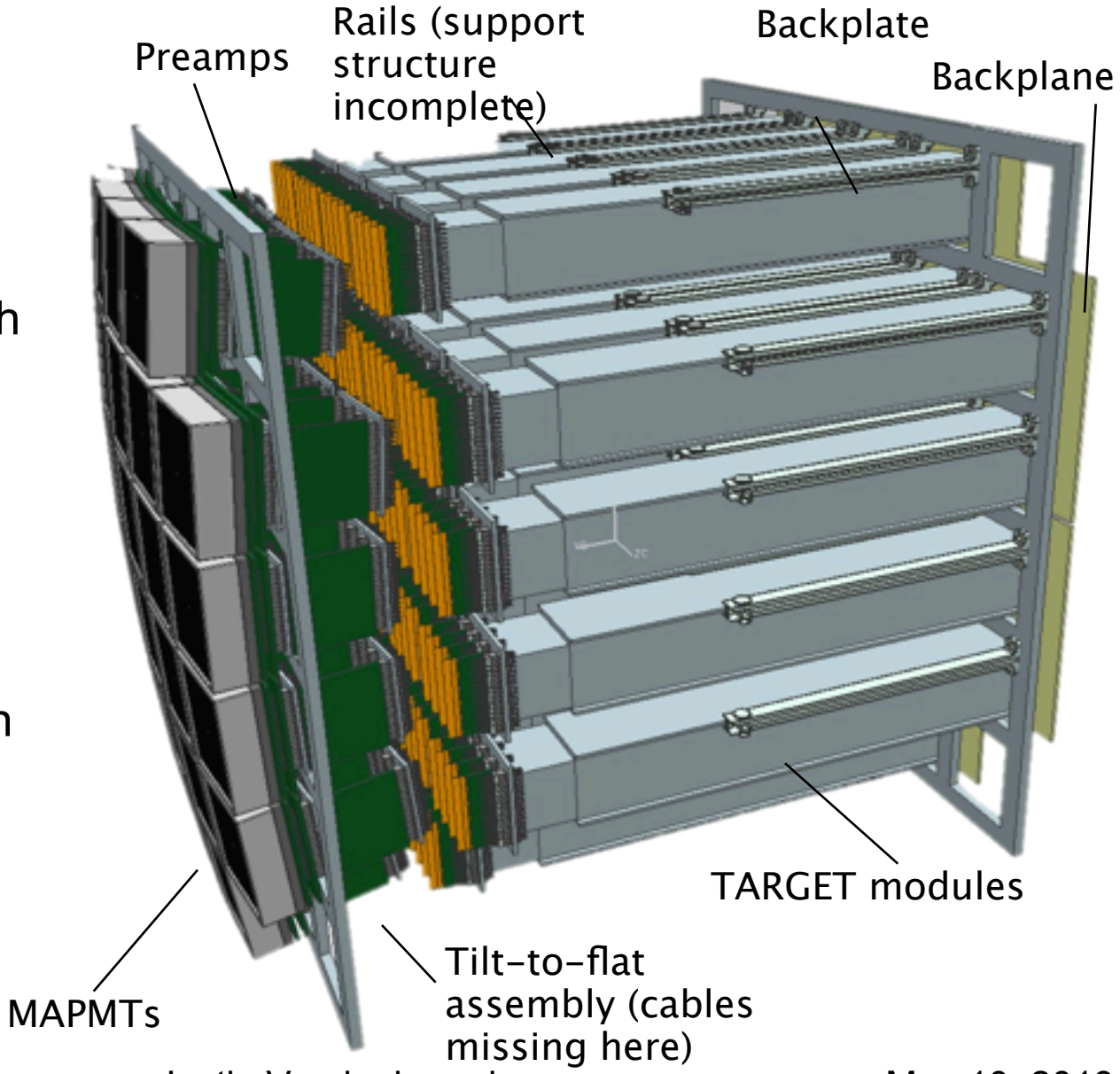
(3) Camera module:



- 2” SiPM
- 64 analog pixels
- 16 trigger pixels
- 4 TARGET chips
- Each pixel is 0.067° (6 mm) square

Modular camera design for Small Size Telescopes

- UK/US/Japan collaboration on "CHEC" (Compact High Energy Camera) for Small Size Telescopes
- Uses SLAC TARGET-based front-end modules
- Will operate on prototype telescopes in France and Sicily



TARGET (v1) design and performance: Astroparticle Physics 36 (2012) 156–165

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TARGET: A multi-channel digitizer chip for very-high-energy gamma-ray telescopes

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ABSTRACT

The next-generation very-high-energy (VHE) gamma-ray observatory, the Cherenkov Telescope Array, will feature dozens of imaging atmospheric Cherenkov telescopes (IACTs), each with thousands of pixels of photo-sensors. To be affordable and reliable, reading out such an array of up to a million channels requires event recording technology that is highly integrated and modular, with a low cost per channel. We present the design and performance of a chip targeted to this application: the TeV Array Readout with GSa/s sampling and Event Trigger (TARGET). This application-specific integrated circuit (ASIC) has 16 parallel input channels, a 4096-sample buffer for each channel, adjustable input termination, self-trigger functionality, and tight window-selected readout. We report the performance of the first-generation version of this chip (TARGET 1) in terms of sampling frequency, power consumption, dynamic range, current-mode gain, analog bandwidth, and cross talk. The large number of channels per chip allows a low cost per channel ($10 to $20 including front-end and back-end electronics but not including photosensors) to be achieved with a TARGET-based IACT readout system. In addition to basic performance parameters of the TARGET 1 chip, we present a camera module prototype as well as a second-generation chip (TARGET 2), both of which have now been produced.

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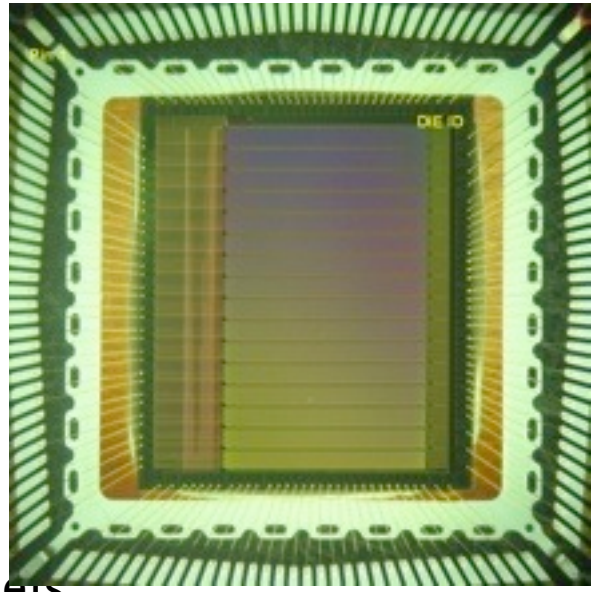
TeV Array Readout with Gsa/s sampling and Event Trigger



- 16 signal input channels
- Analog sampling and storage (switched capacitor array)
- Primary / sampling buffer consisting of 64 cells per channel
- Secondary / storage buffer consisting of 16,384 cells per channel
- Analog samples are digitized when desired, based on internal or external trigger decision
- At 1.0 GSa/sec, 16 μs buffer enables
  - large latency for backplane + array trigger to make a readout decision
  - ability to buffer multiple hits for dead time-free operation

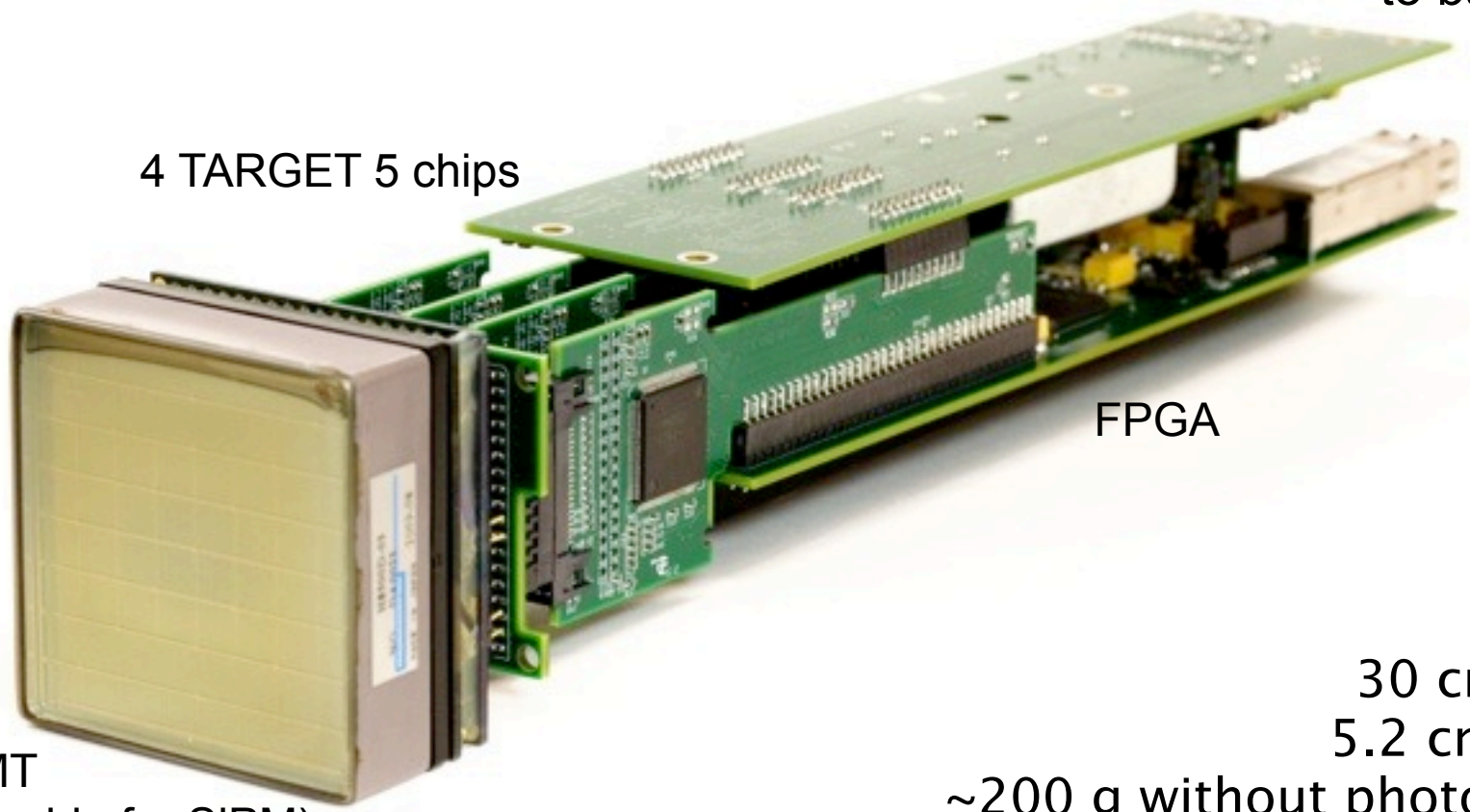
Key features of the TARGET chip

- Self-triggering: no need for parallel circuitry to provide trigger
- >10 bits (effective, after noise subtraction)
- Fast sampling: 1 GSa/sec
- High channel density (16 channels per chip) for low cost, power, size, and weight per channel
- Deep buffer: 16,384 cells (16 us) to allow time for trigger decision and multi-hit buffering (zero dead time operation)
- High analog bandwidth (400 MHz)
- Highly configurable: user can choose tradeoff between resolution, range, digitization time

TARGET 5 features

Specification	value
Channels	16
Storage cells per channel	16,384
Pre-amplifier?	No
Single-ended or (pseudo) differential?	SE
Bandwidth (MHz)	~380 MHz
Cross talk @ 3 dB frequency	<1%
AC saturation?	No
Internal/external control voltages	Int
Trigger	4 ea. analog sum
Wilkinson ADCs (ch x samples)	16 x 32
Dead time for 10 bit, 16 ch, 48	10
Sampling frequency (GSa/sec)	0.2-1.4
Effective dynamic range (bits)	11.0

Camera module with 4 TARGET 5 chips to read out 64 channels

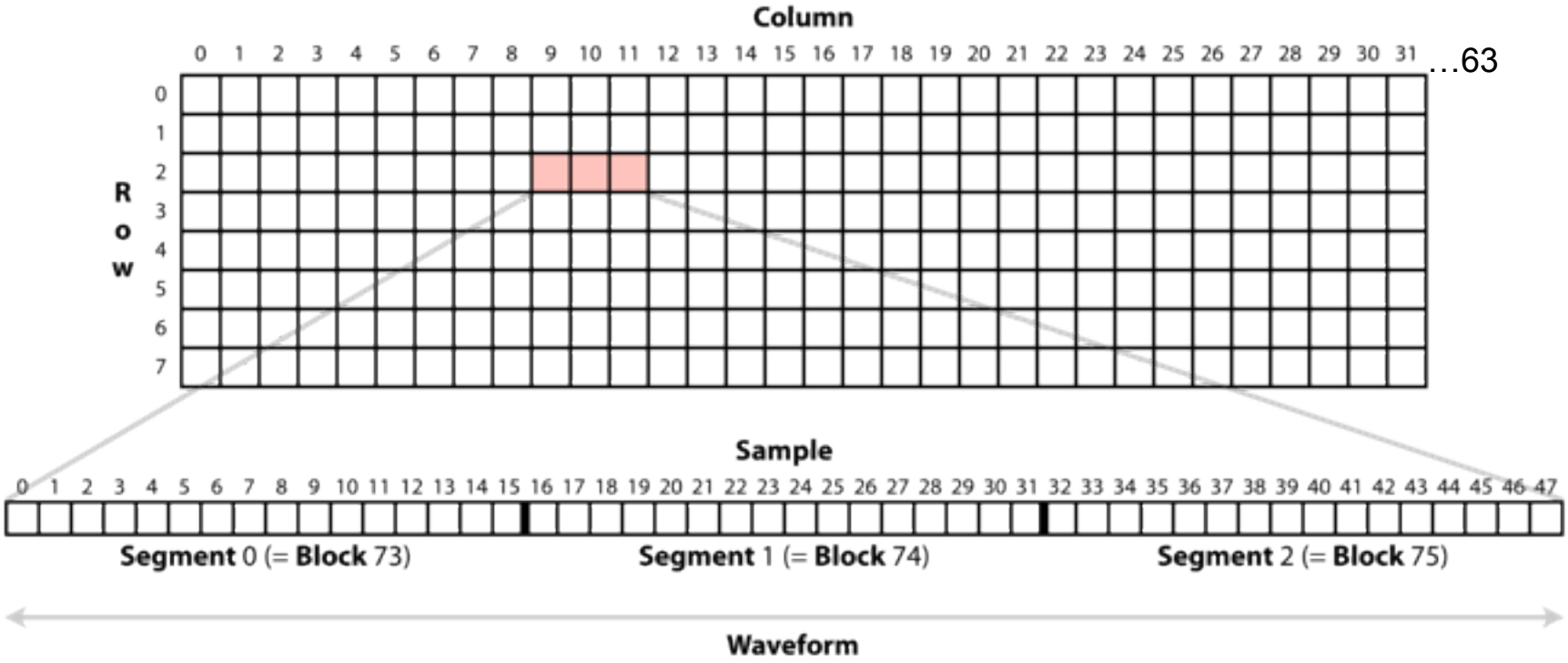


30 cm length
5.2 cm square
~200 g without photo-sensor
7 W for 64 channels (not including photo-detector)

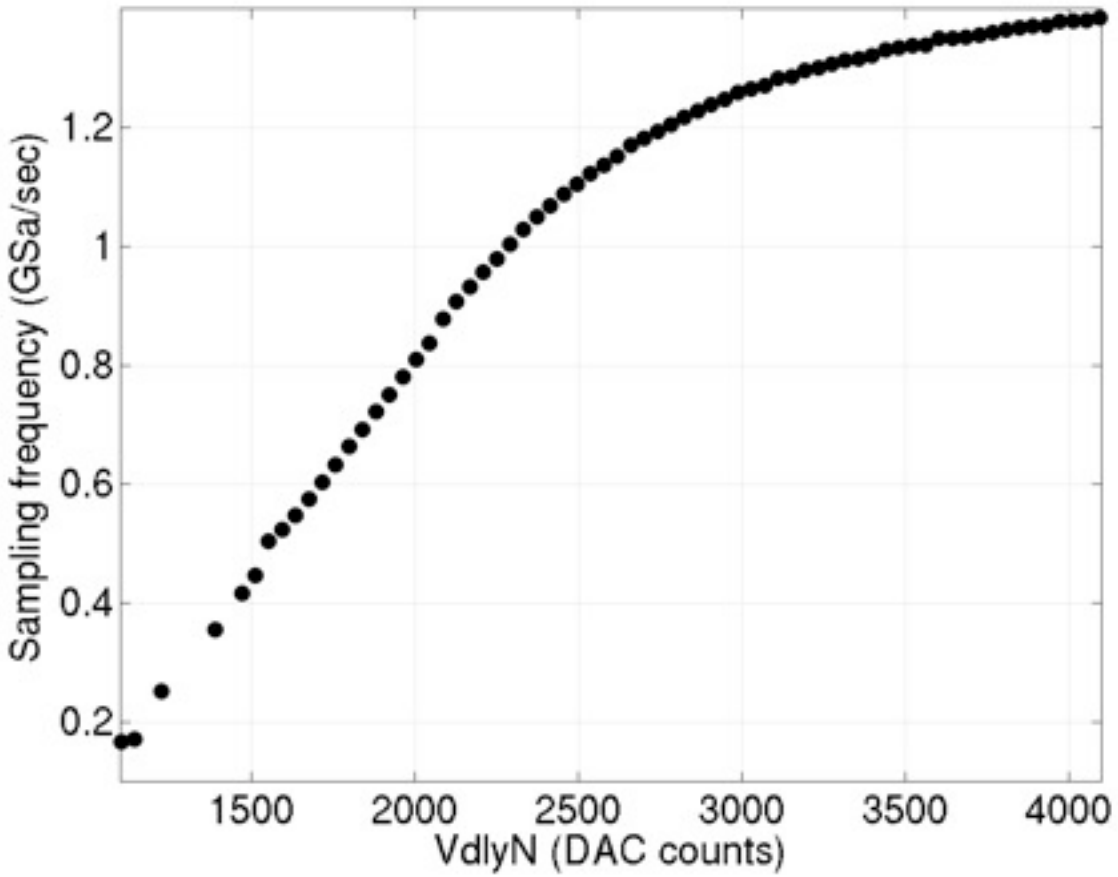
Evaluation board

- 1 FPGA, 1 TARGET chip, 5 V power, fiber (to ethernet) interface

Analog sampling and storage in switched capacitor array (16,384 cells per channel)

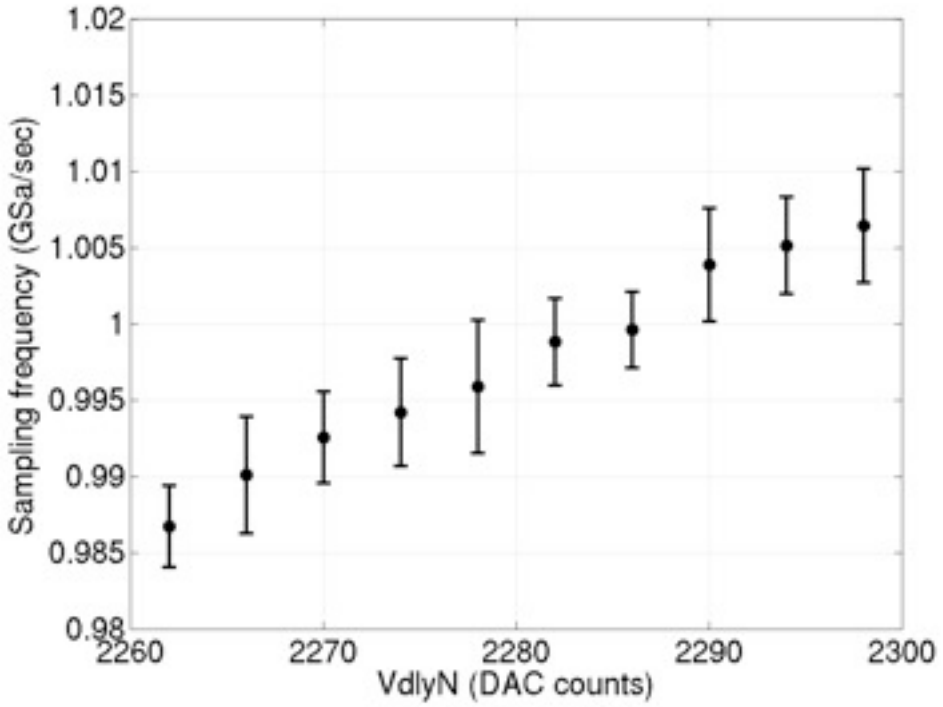


Sampling frequency tunable between ~0.2 and ~1.4



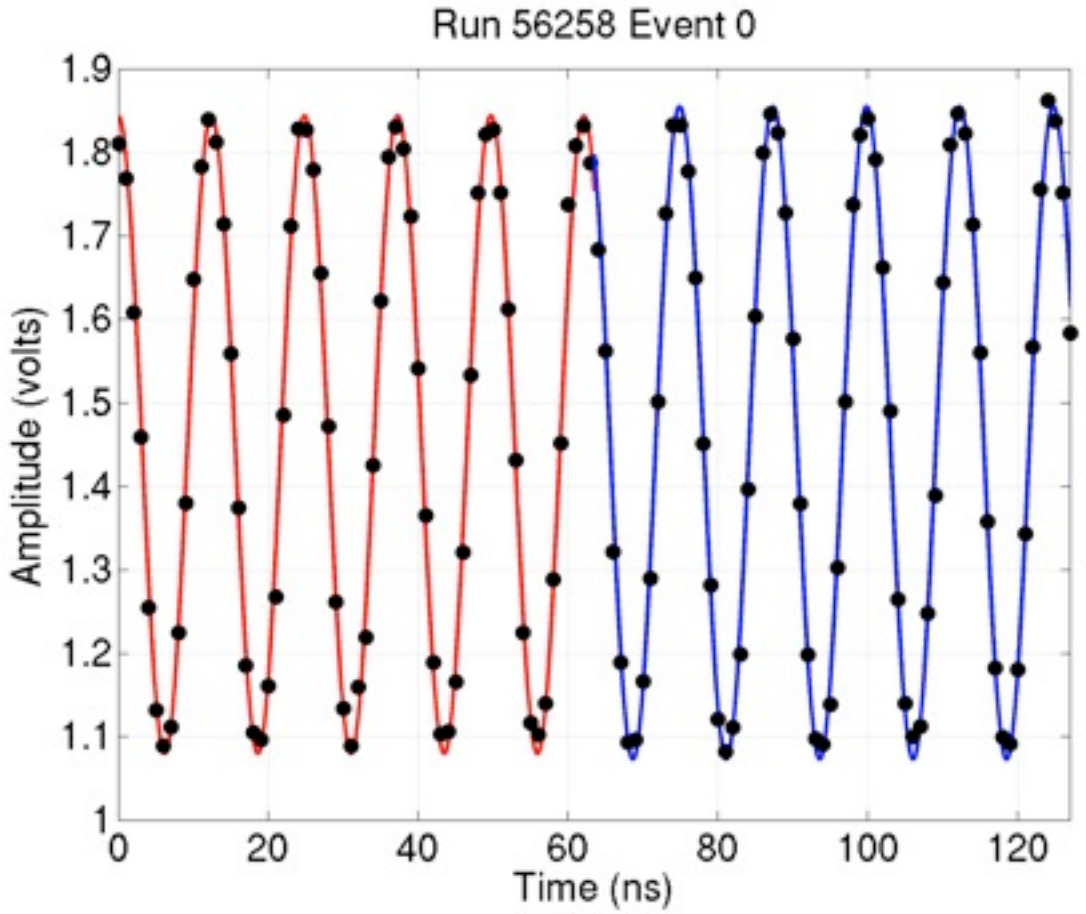
- To maintain phase lock, 64 samples should be a multiple of 8 ns (125 MHz FPGA clock), so sampling frequency should be (8 GSa/sec)/N where N is integer
- Possible frequencies (GSa/sec): 1.33, 1.14, 1.00, 0.89, 0.80, 0.73, 0.67, 0.62, 0.57, 0.53, 0.50, 0.47, 0.44, 0.42, 0.40, …

Fine control of sampling frequency



- Fine control of this parameter achieves stable, phase-locked, temperature-independent sampling:
  - Lock sampling frequency to a clock on FPGA
  - Maintain frequency and phase across 32-sample blocks (edges of FPGA timing signals)
  - Compensate for temperature variation in ASIC sampling oscillator

Demonstration of phase locking across block

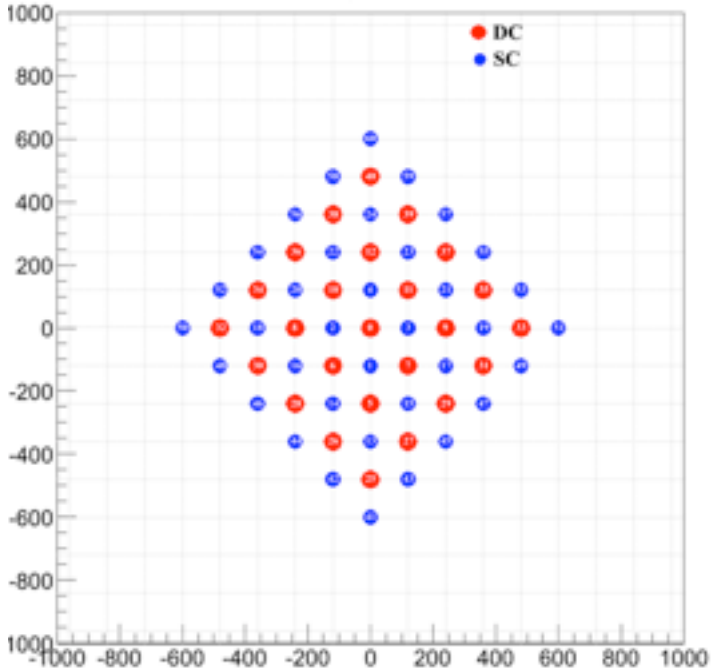


- 80 MHz sinusoid sampled at 1 GSa/sec
- From first block of 64 samples to second, sampling phase is aligned to ~0.1 ns

CTA trigger chain

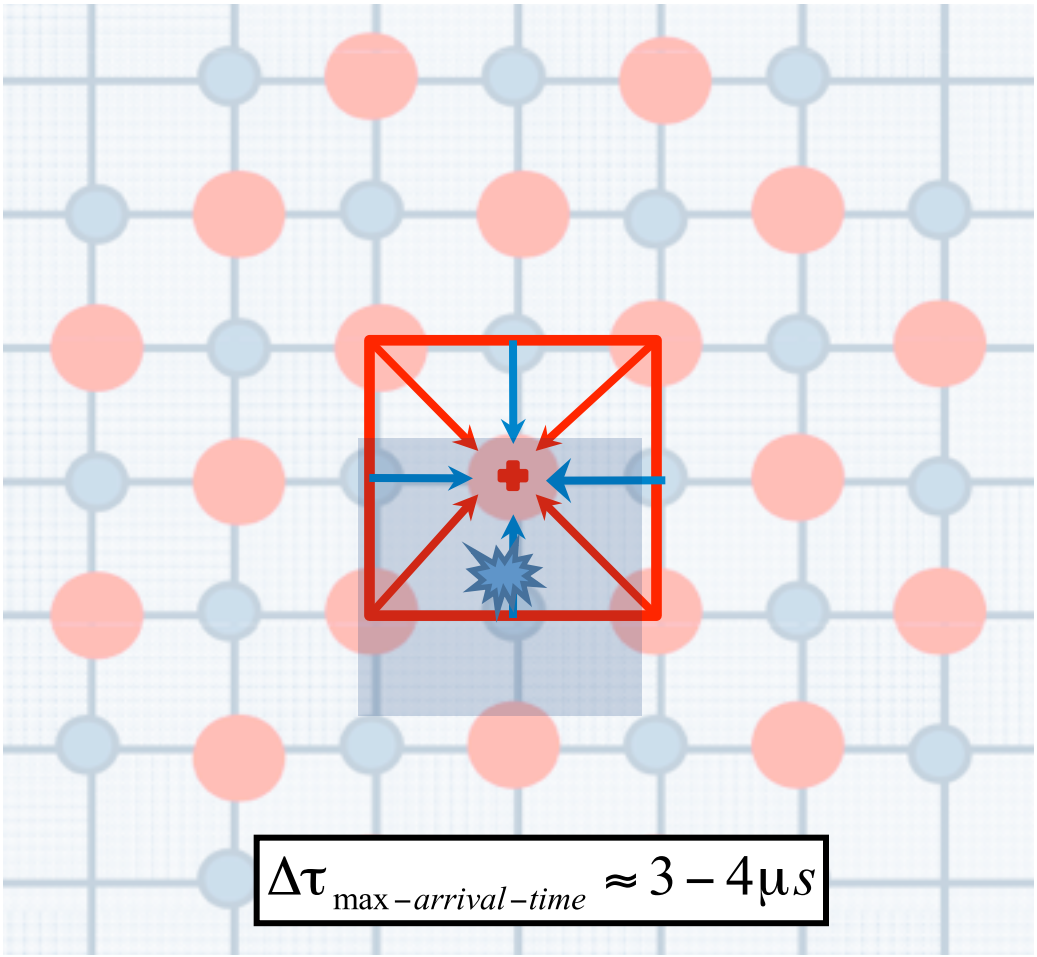
1. Pixel level: Discriminator applied to individual trigger pixels (each trigger pixel is analog sum of 4 analog pixels)
2. Camera level: multiplicity and topology of pixels in camera (programmable in firmware)
3. Array level: coincidence between neighboring telescopes (programmable in firmware)

- Once array trigger is satisfied, readout command is sent back to TARGET
- Timing synchronized across array to 2 ns



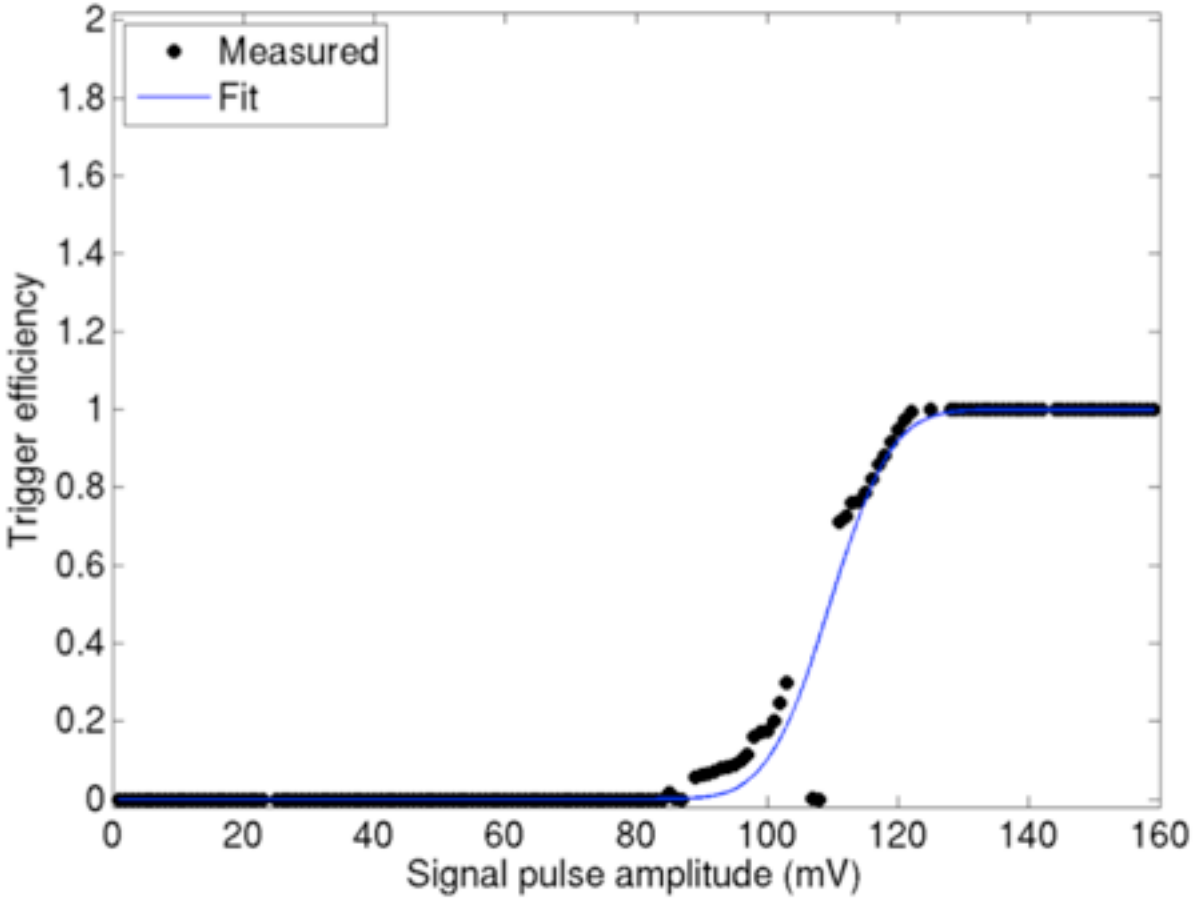
Distributed array trigger

9 (8+1) telescope hybrid (5+4) cell



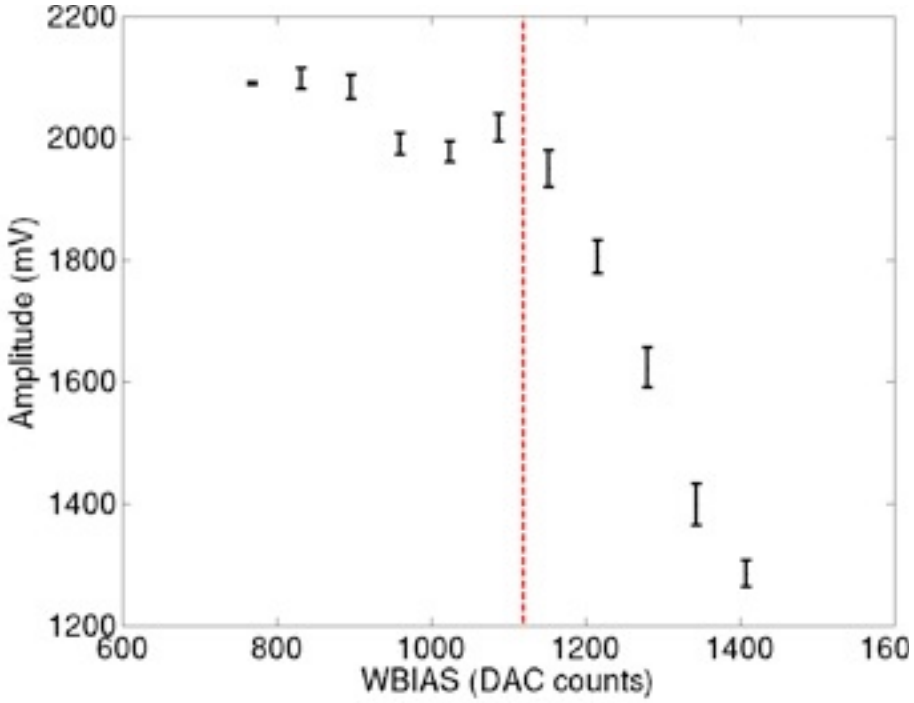
- Every telescope acts as its own array trigger
- Information from neighbors flows to telescope
- Readout command delivered locally
- Multiplicity/ topology-based array trigger

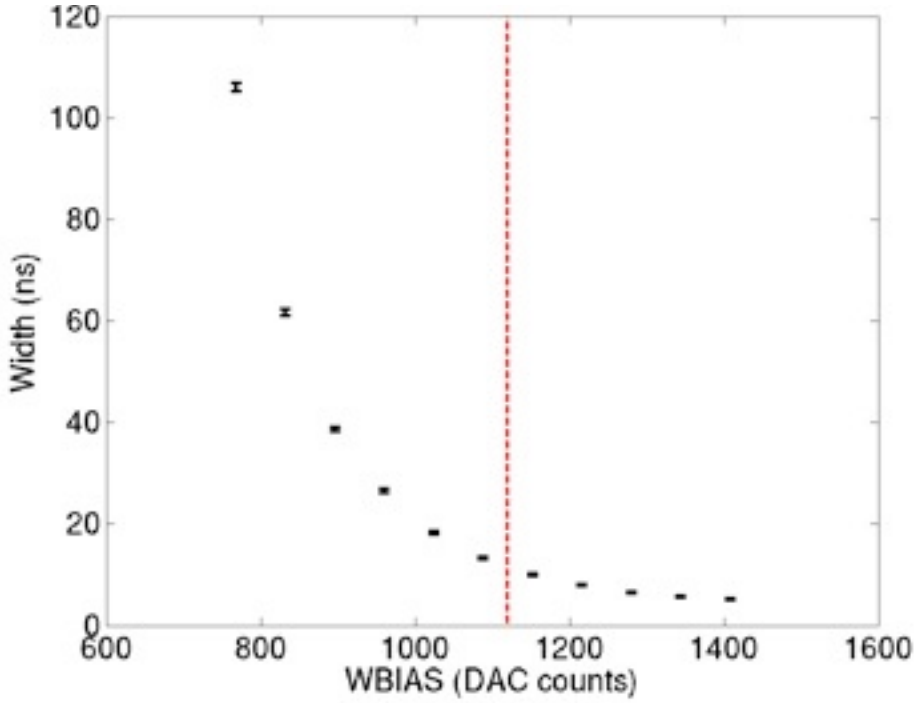
Trigger performance



- 5 triggers available: 4 ea. analog sum of 4 channels, 1 ea. analog sum of 16 channels
- Trigger performs well except cannot set threshold below 25 mV (6 photo-electrons)
- Will try to lower this in TARGET 7

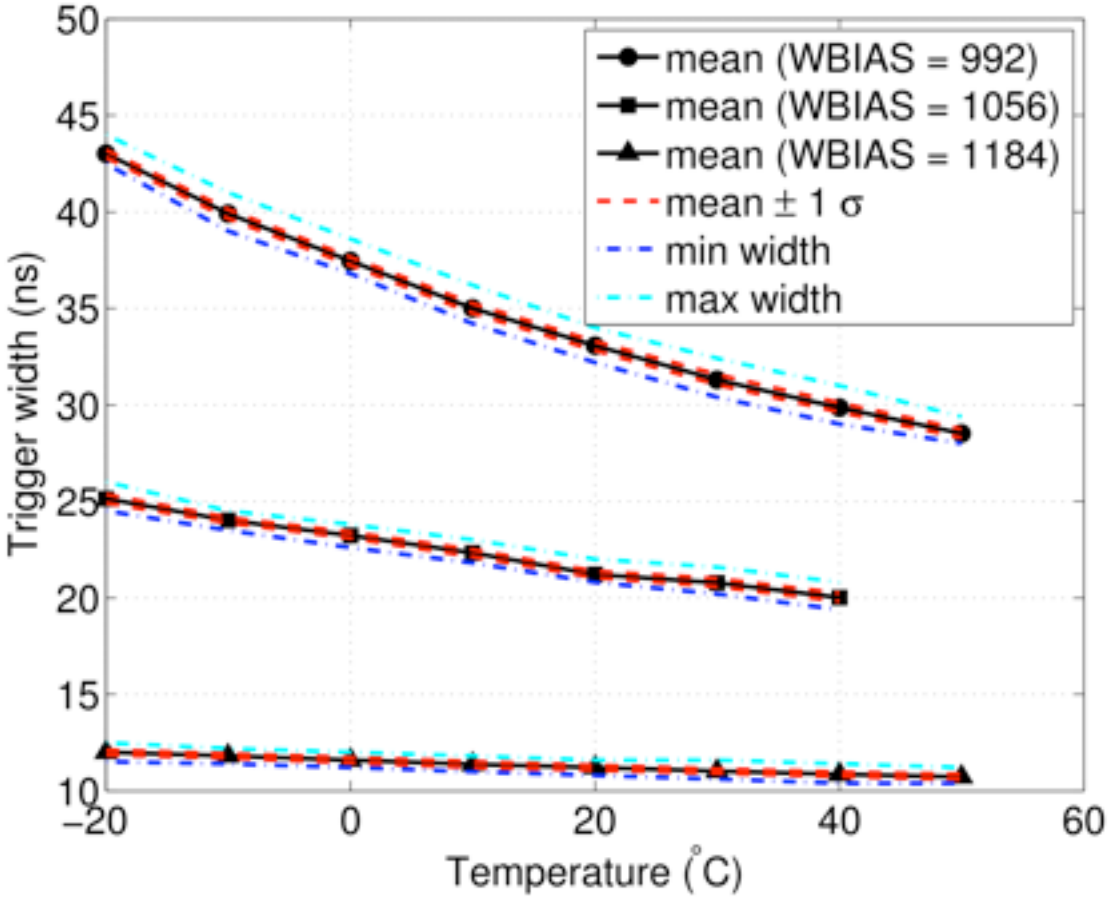
Amplitude and width of trigger signal vs. control voltage (WBIAS)





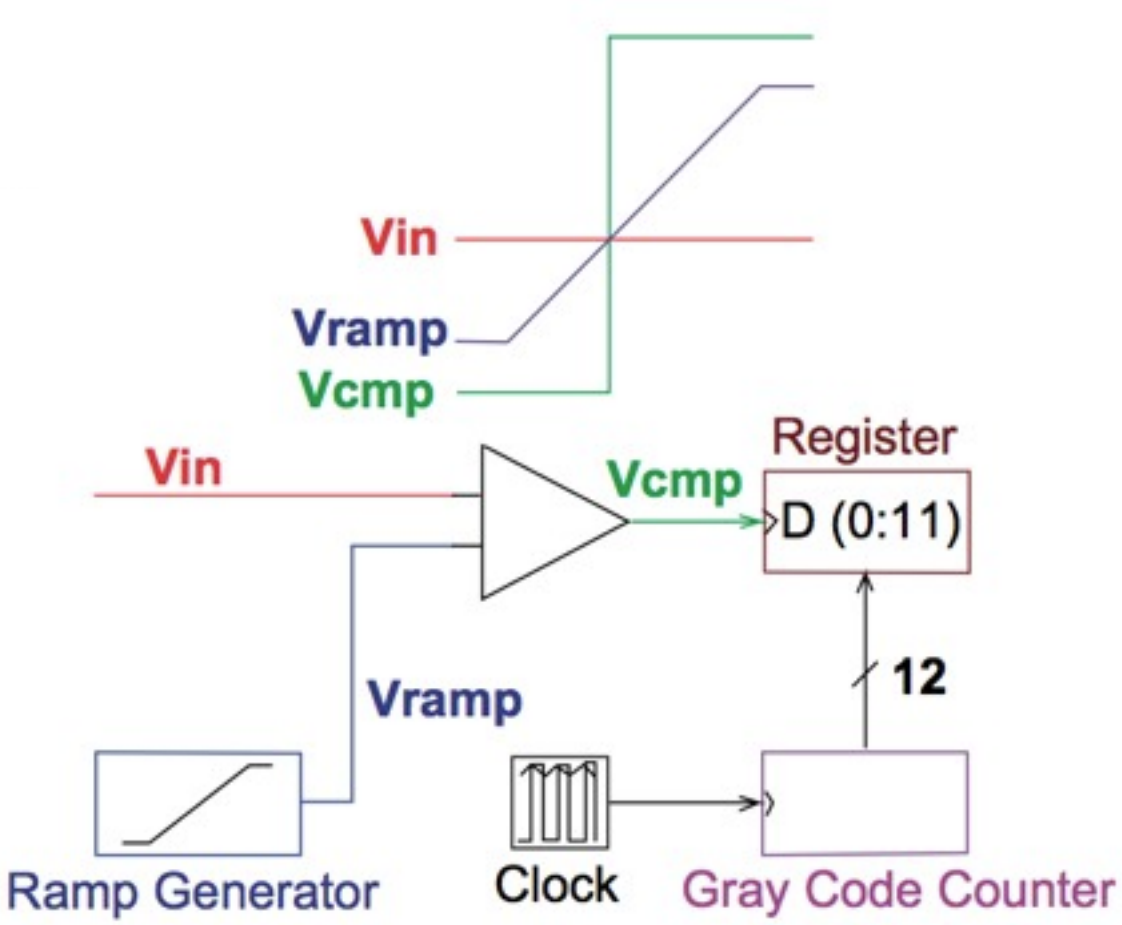
- Can achieve trigger signal amplitude > 2 V for width >10 ns

Temperature variation of trigger width



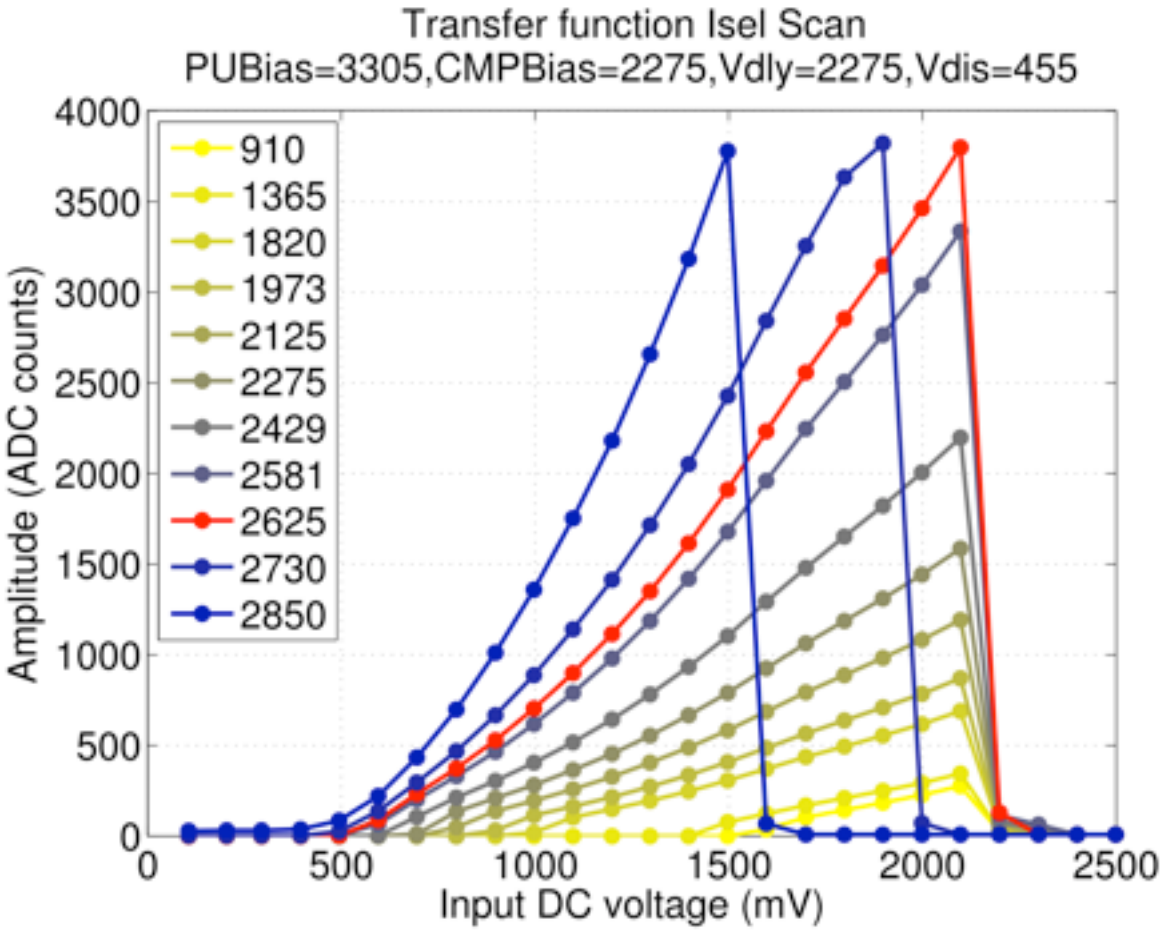
- Width is stable for the narrow (~10 ns) trigger signals we will use
- Stabilization with a feedback loop in FPGA could be implemented if necessary

After analog sampling and trigger decision, digitization is performed with Wilkinson analog to



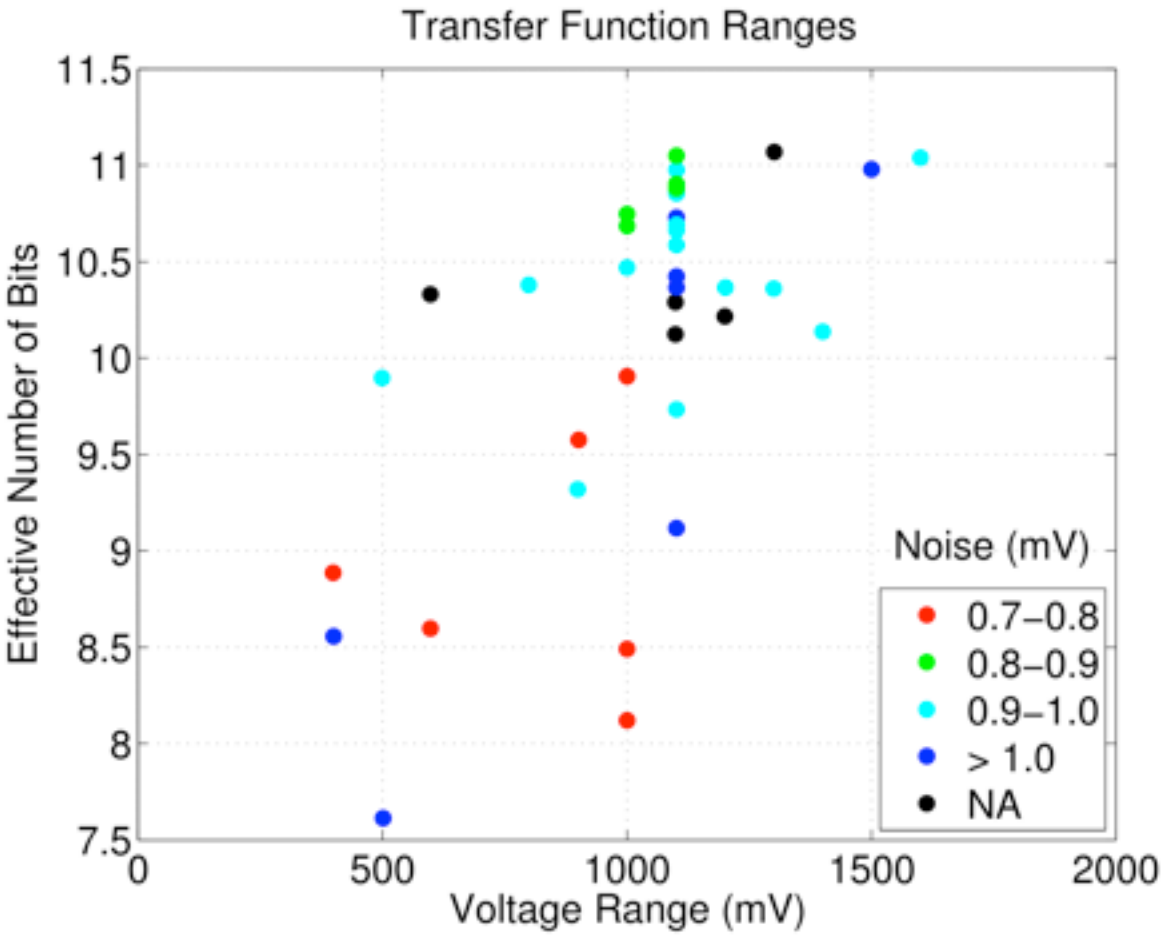
G. S. Varner et al. NIM A 583 (2007) 447

User-tunable transfer function

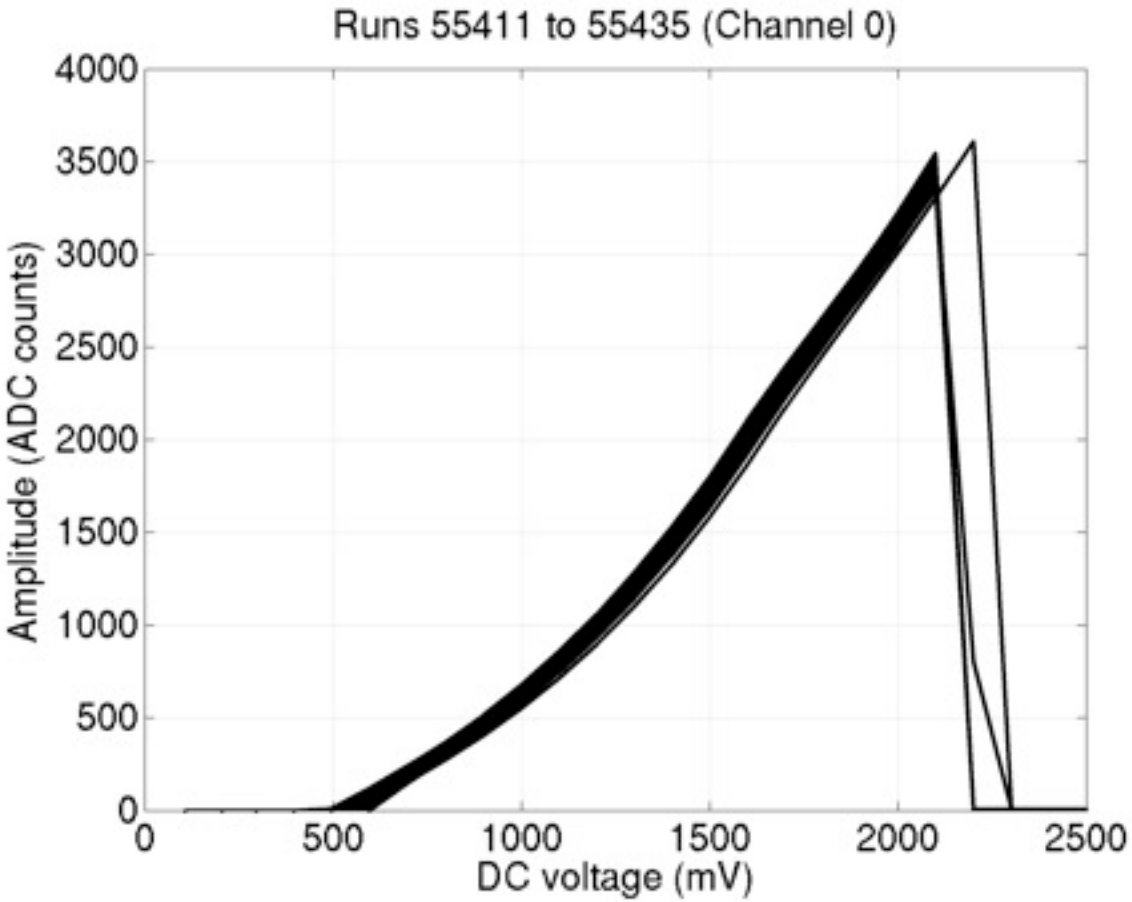


- User can choose desired optimization of dynamic range, resolution, dead time

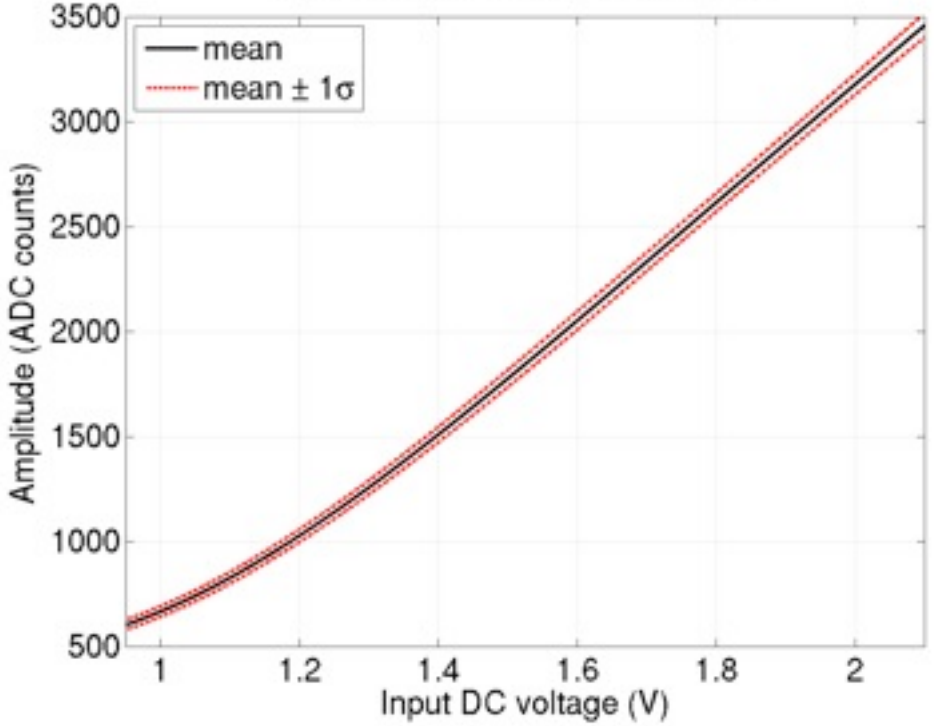
Configurable to choose combination of range, resolution, noise, and digitization time



Transfer functions for 64 individual storage

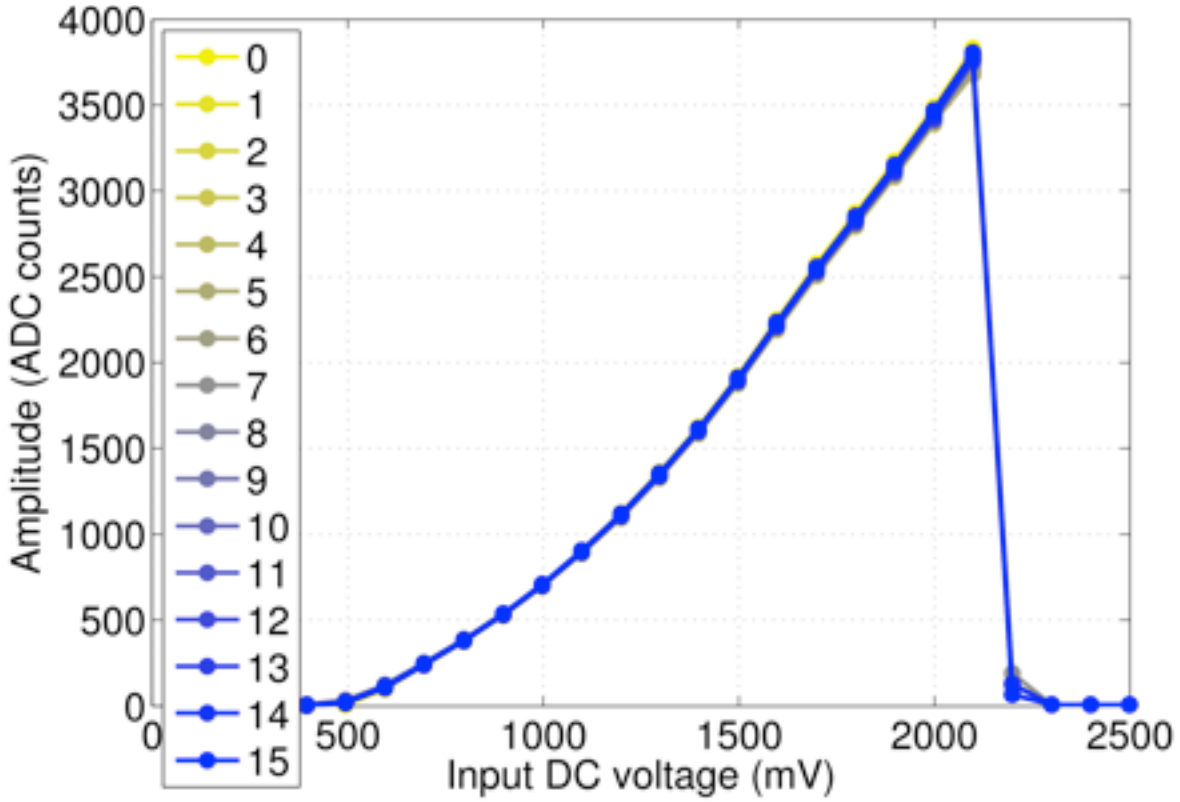


TARGET 5 transfer function, noise, dynamic



- Configurable for desired voltage range; example shown for one configuration
- Red curves indicate ±1 sigma variation among 544 storage cells
- Voltage input range: 948 to 2149 mV (1.2 V)
- ADC range: 604 to 3596 counts
- ADC dynamic range: 2993 counts (11.5 bits)
- Noise (average for input signals 1.0 to 2.1 V, 1 sigma): 0.6 mV = 1.4 ADC counts = 0.5 bits
- Effective dynamic range (subtracting noise bits): 11.5 – 0.5 = 11.0 bits (cf.

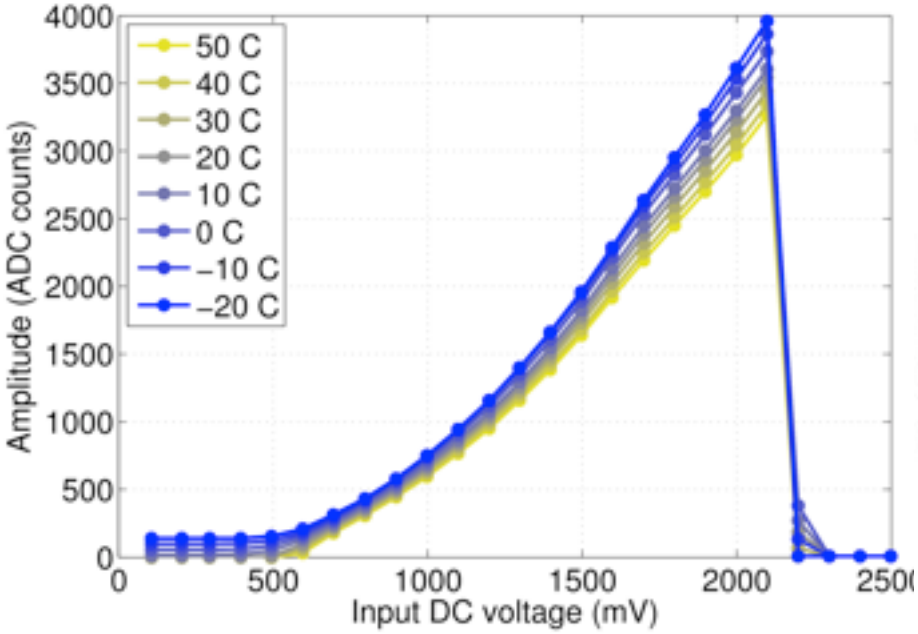
Channel-to-channel transfer function variation



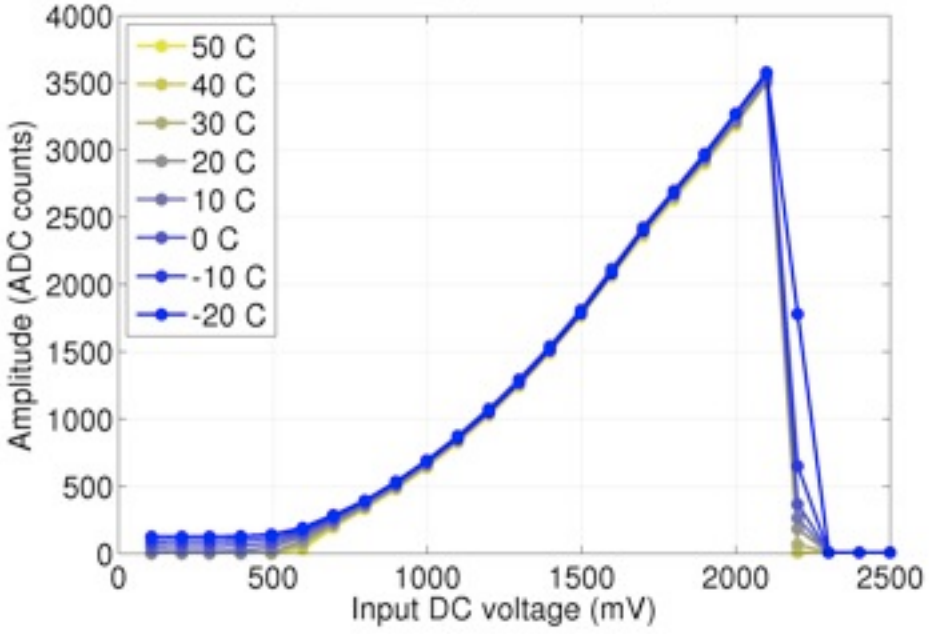
- Each curve is average of first 64 storage cells
- Channel-to-channel variation smaller than cell-to-cell variation

Temperature variation of transfer function: significantly reduced with Wilkinson frequency feedback loop

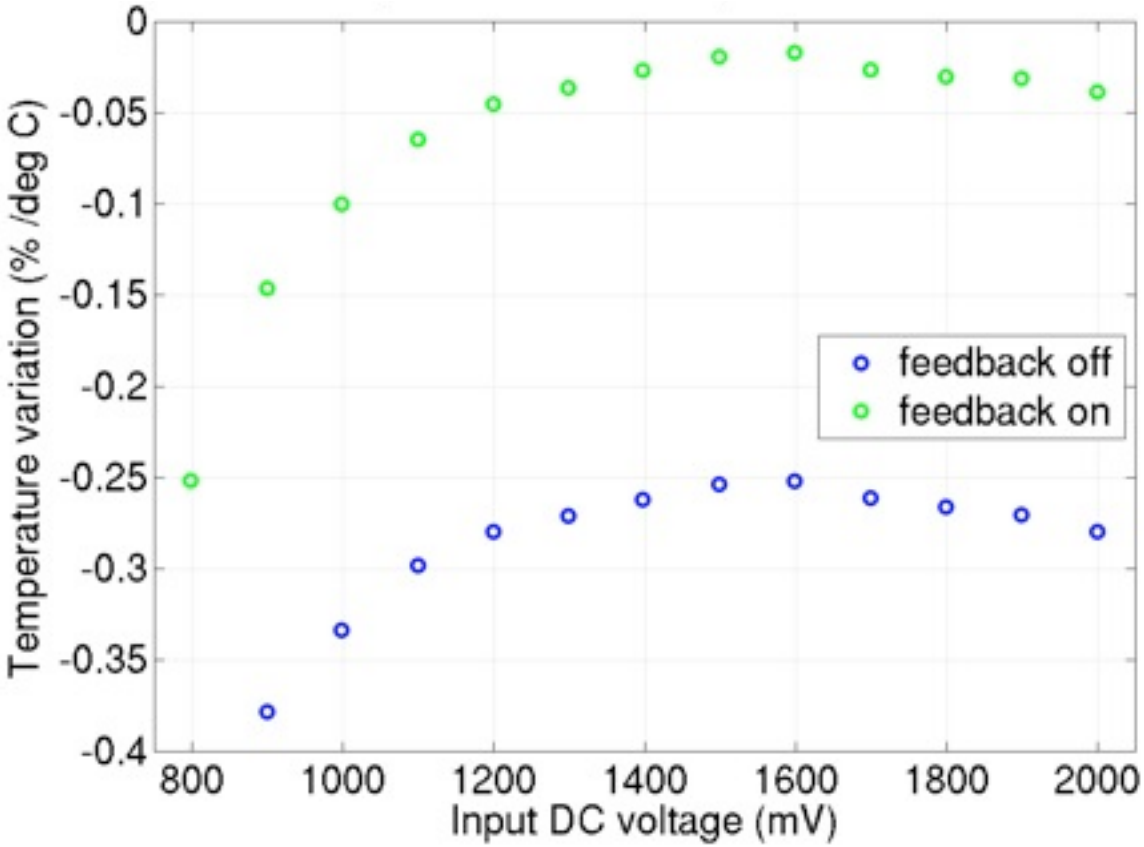
Feedback loop off:



Feedback loop on:

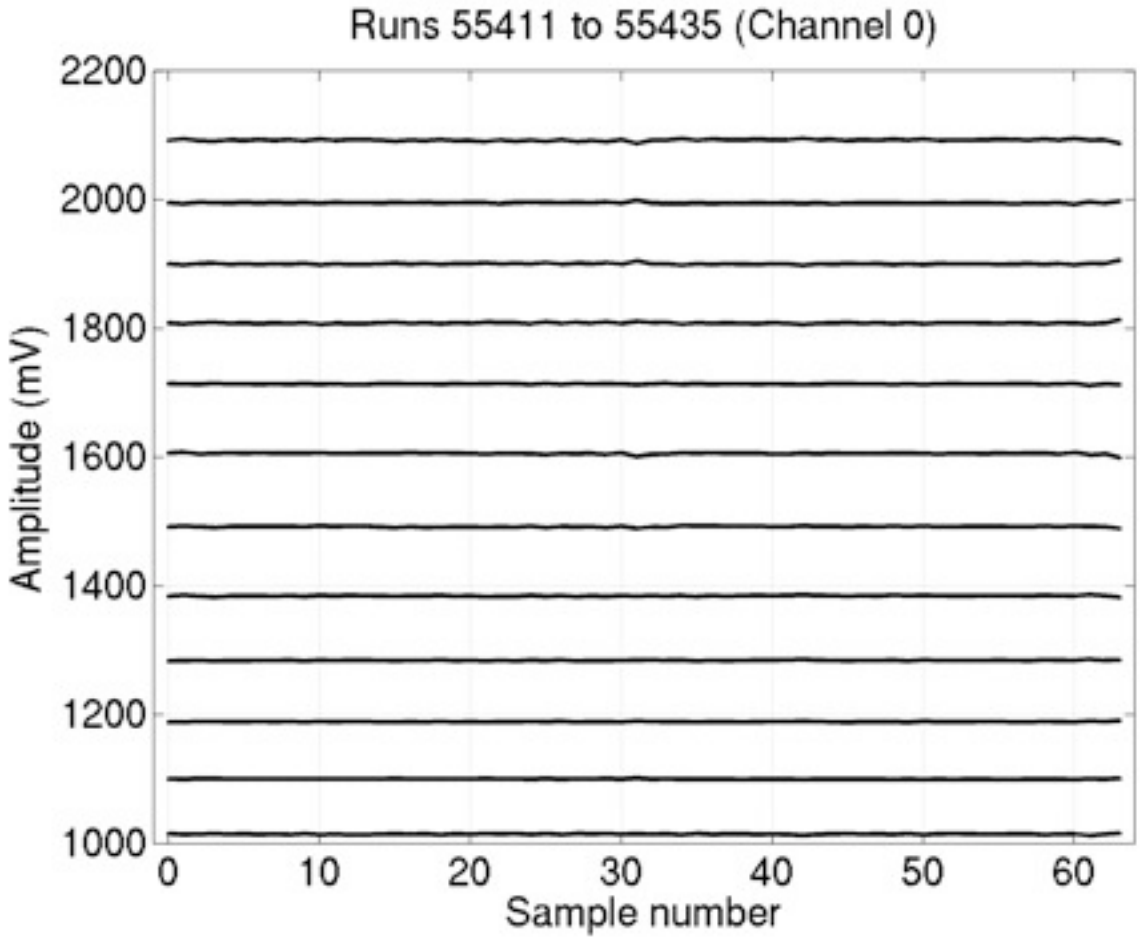


Feedback loop decreases temperature variation of transfer function



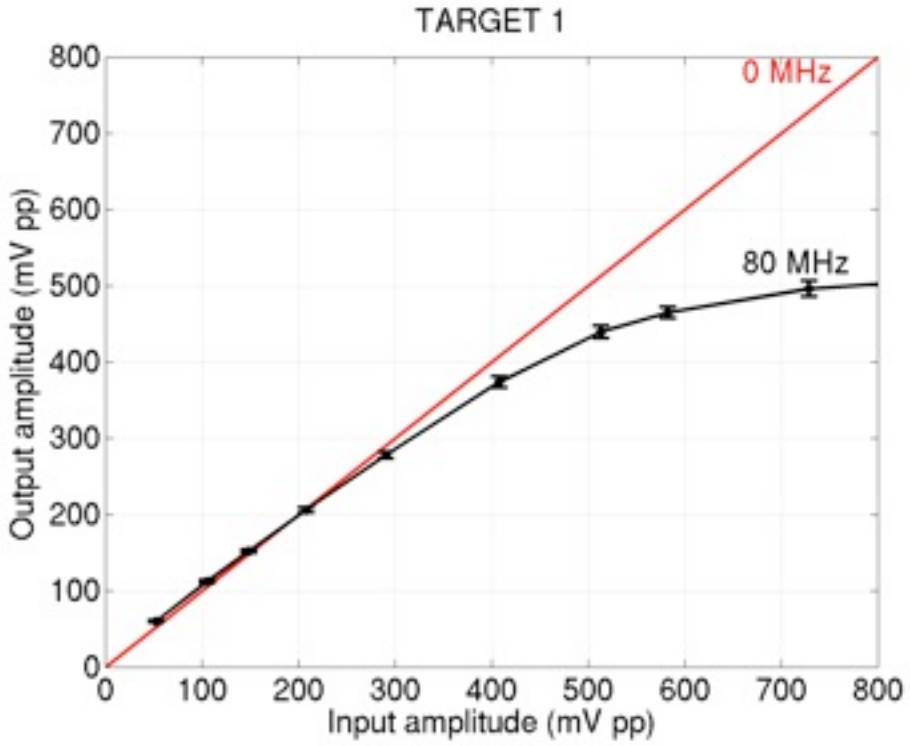
- Feedback loop decreases temperature variation from ~0.3 %/°C to ~0.05 %/°C

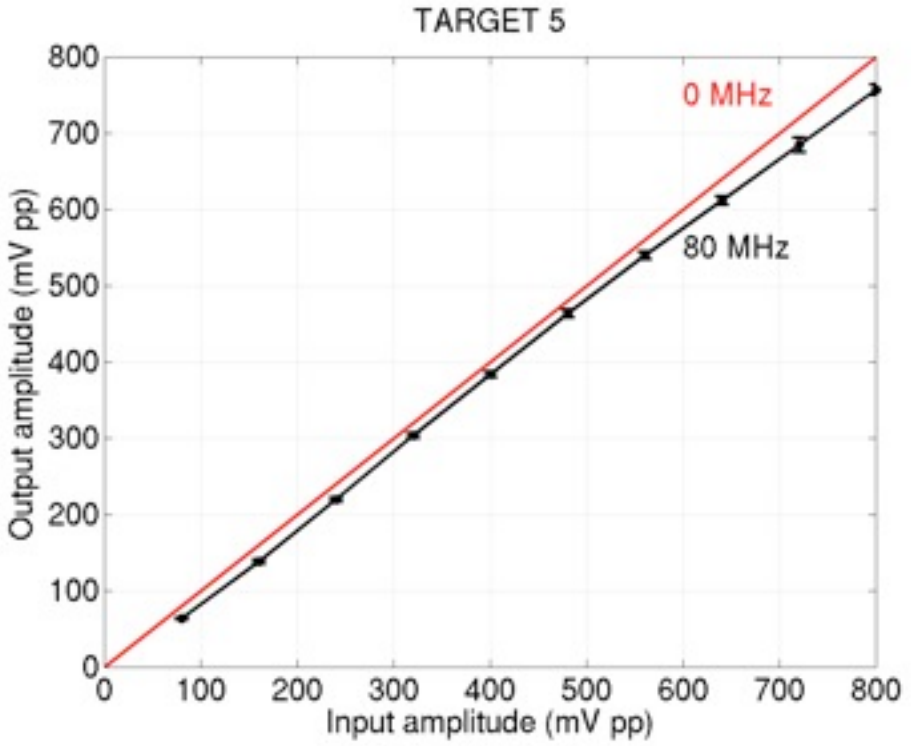
Calibrated DC waveforms every 0.1 V from 1.0 to 2.1 V



- Cell-dependent calibration has been applied
- 12 waveforms overlaid

AC linearity





- AC saturation was present in TARGET 1 and is fixed in TARGET 5

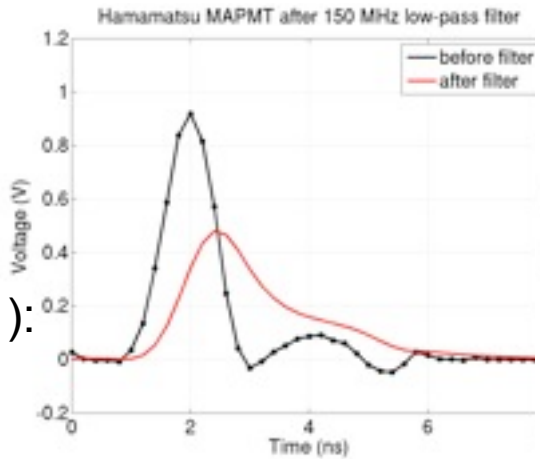
Calculated SiPM pulse shapes with TARGET

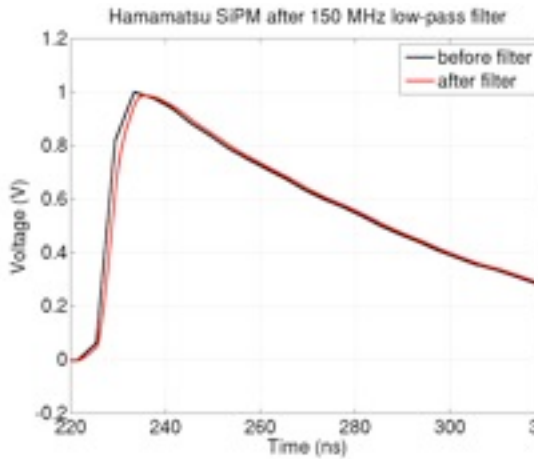
Hamamatsu MAPMT:

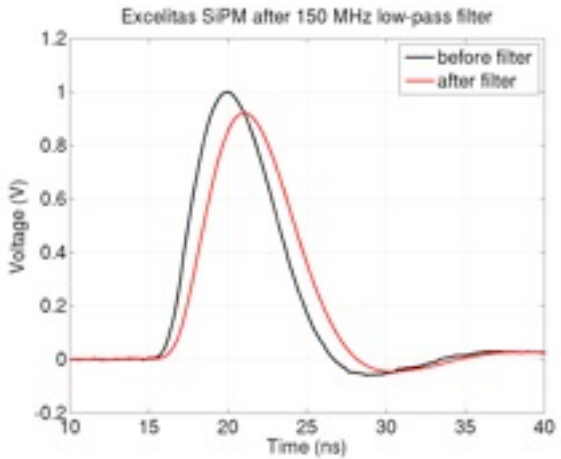
Hamamatsu SiPM:

Excelitas SiPM:

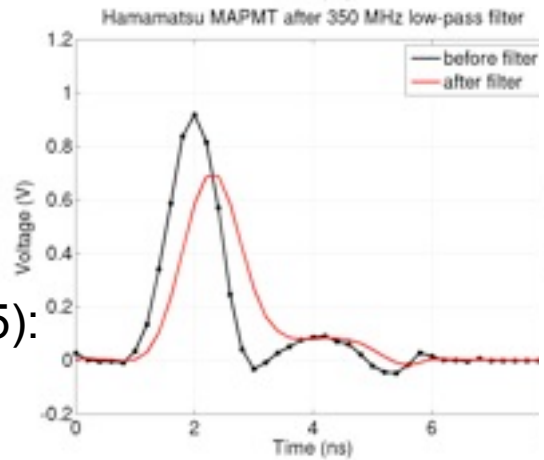
150 MHz bandwidth (TARGET 1):

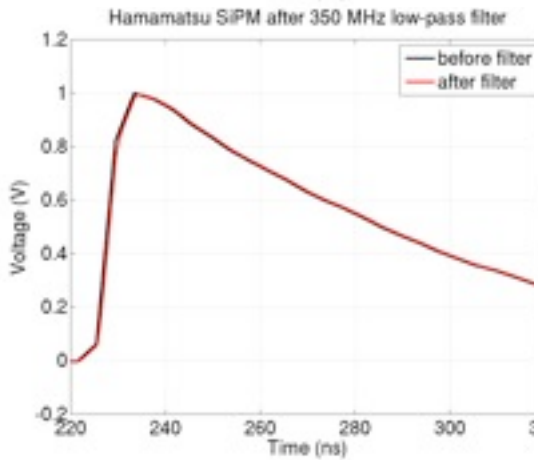






350 MHz bandwidth (TARGET 5):





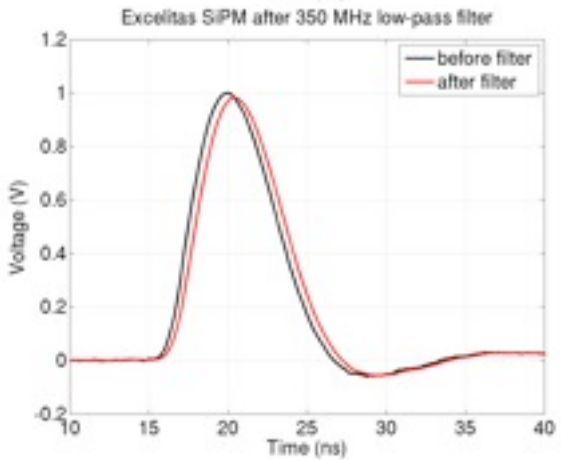
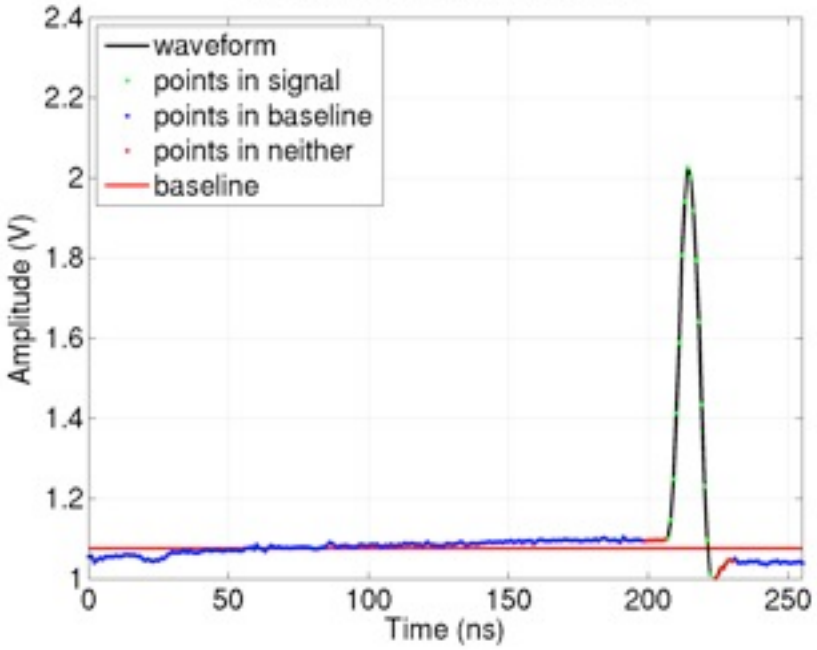
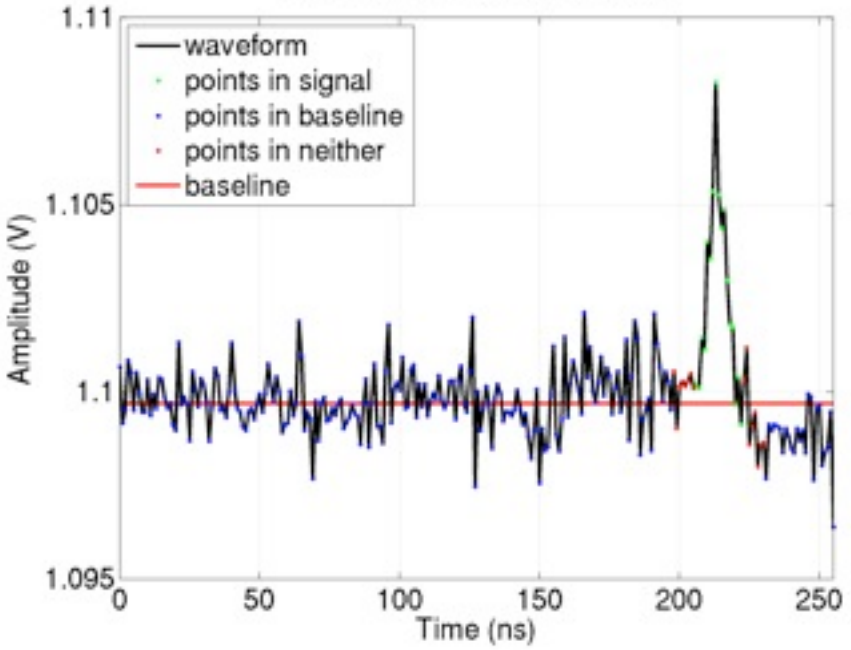


Photo-electron pulses simulated with electrical pulses

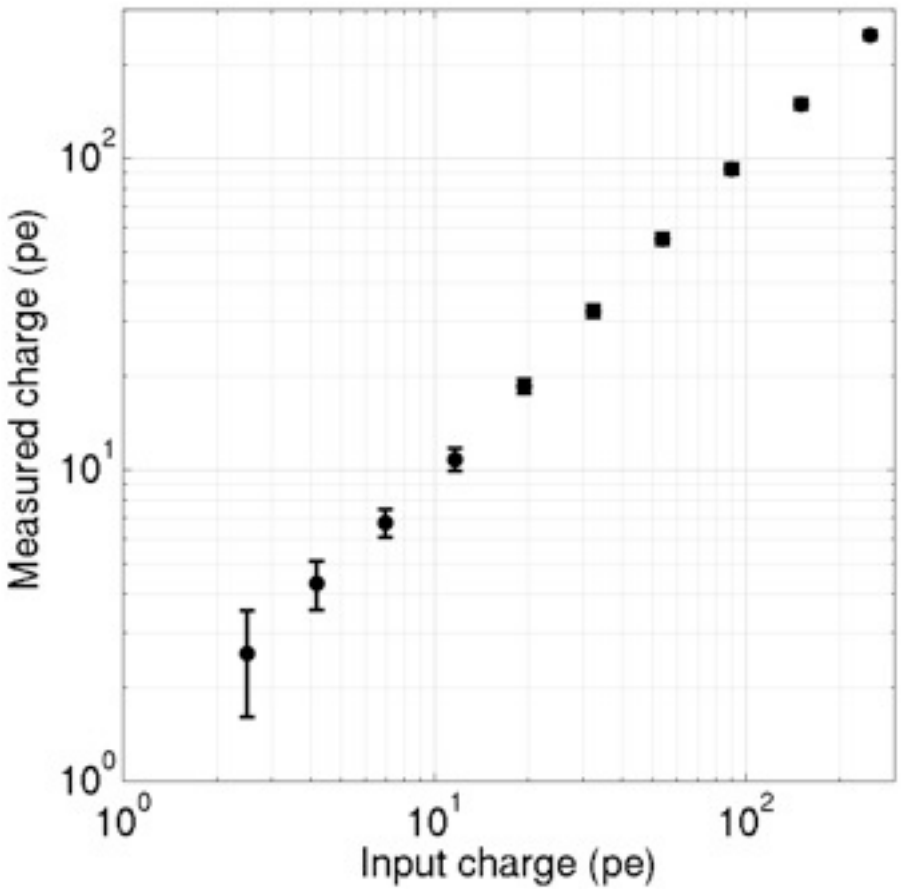
1 V pulse
equivalent to 250 photoelectrons



10 mV pulse
equivalent to 2.5 photoelectrons

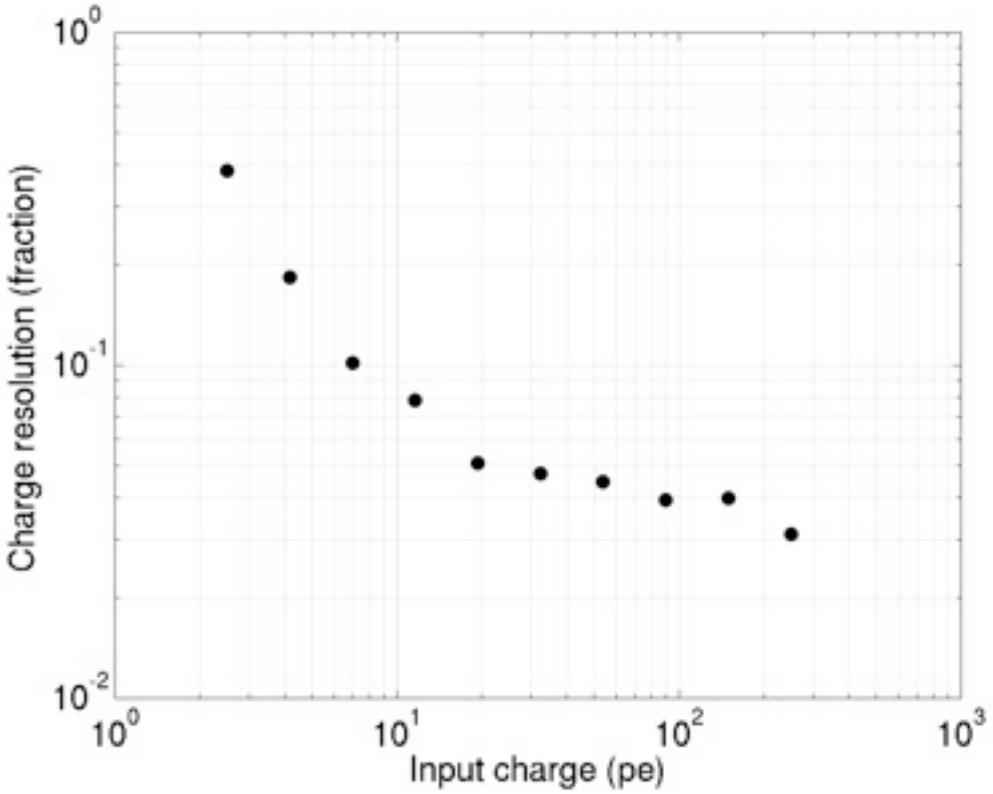


Charge measurement with simulated photo-electron pulses



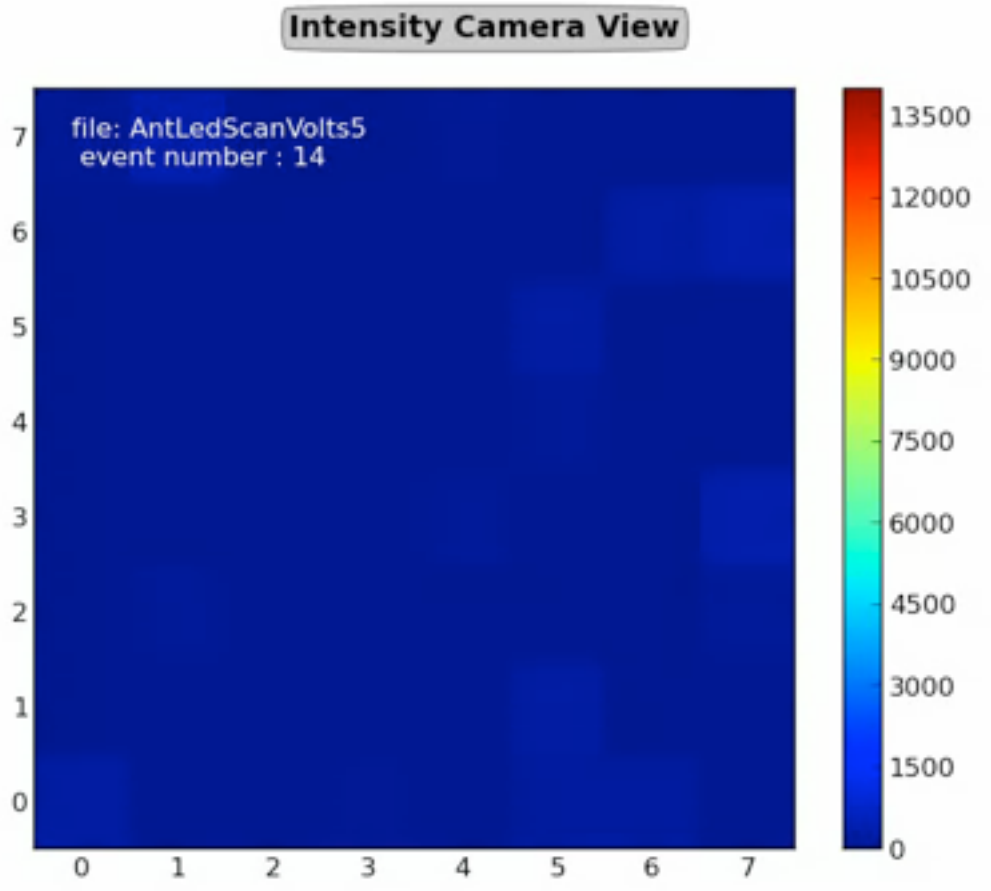
- Integrated charge determined by summing 16 samples

Charge resolution



- Achieves 3% resolution at 250 photo-electrons, 40% resolution at 2.5 photo-electrons
- Work in progress to measure 1 photo-electron resolution and to reduce noise for better performance at low charge
- This measurement includes only contribution due to TARGET noise
- Additional contributions: photo-detector noise, cross-talk, after-pulses, gain uncertainty

TARGET 5 camera module: “first light” movie



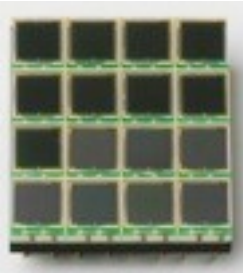
- MAPMT (8 x 8 pixels) illuminated by LED
- LED intensity increased over time
- Using un-calibrated ADC counts (results in large pixel to pixel variations)

Conclusion and outlook

- CTA groups busy building prototypes, including the first-ever Schwarzschild-Couder telescope
- Modular TARGET-based front-end readout system enables use with both Medium Size and Small Size telescopes
- Newest TARGET chip, version 5 (fabricated in Fall 2012) is performing well
- Small design improvements will be made to both chip (TARGET 7, esp. trigger) and module before producing 25 front-end modules for US prototype (medium-energy camera) and 32 for UK prototype (high-energy camera)
- TARGET could be interesting for any experiment that records ~10-1000 ns waveforms sampled at ~1 GSa/sec with deep (16 us) buffer, self triggered and highly integrated for low cost, power,

Additional slides

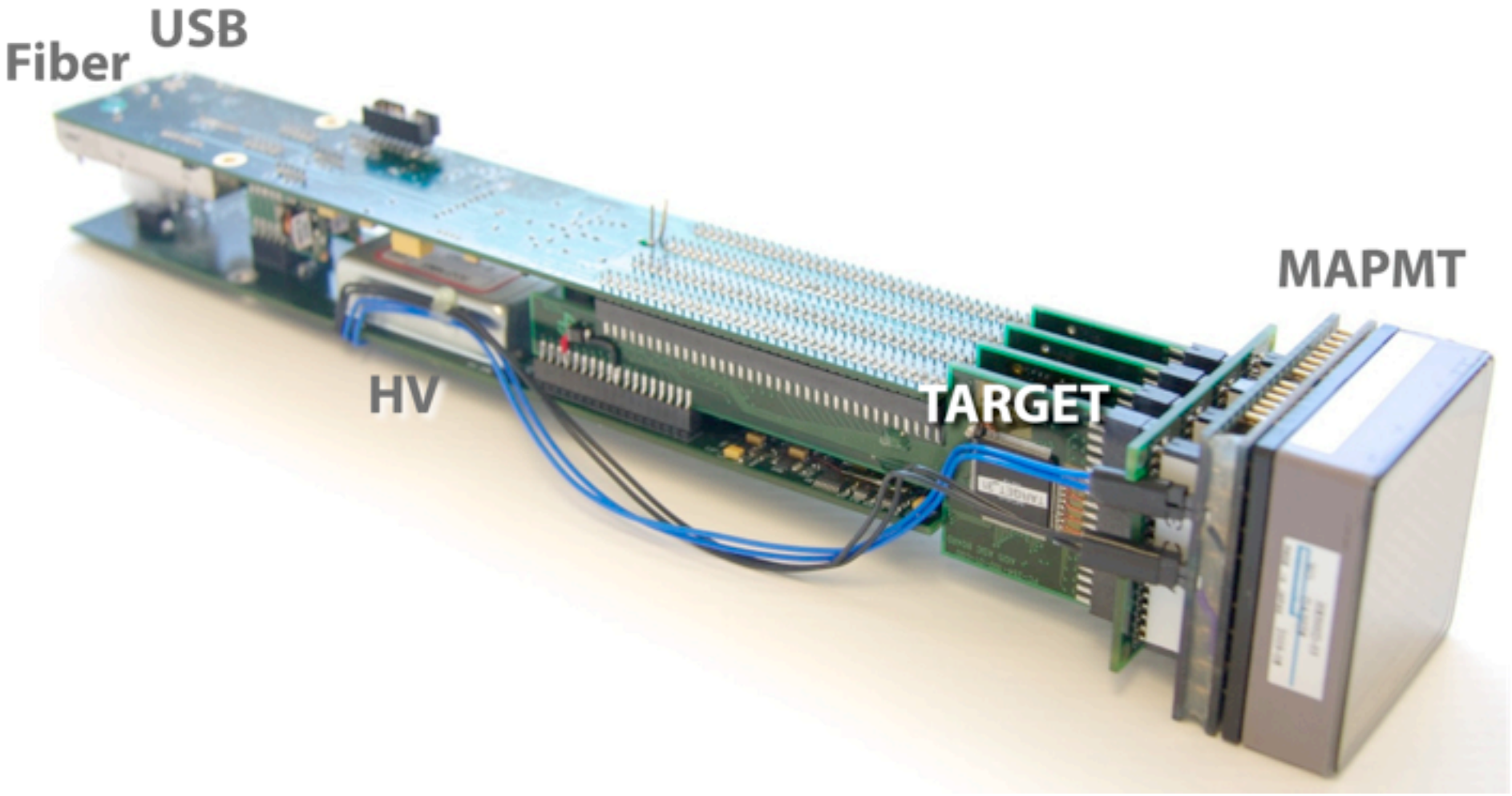
Silicon photomultipliers



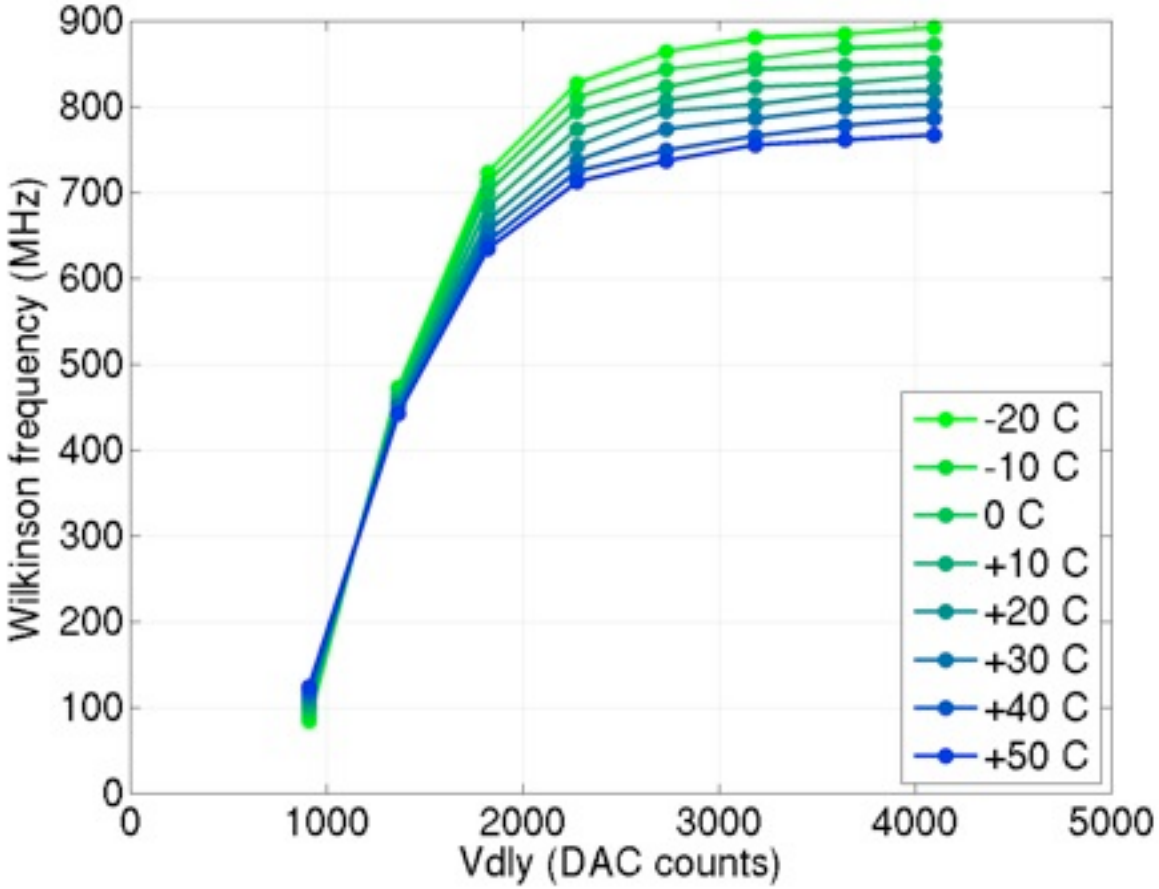
Hamamatsu S11064-050P

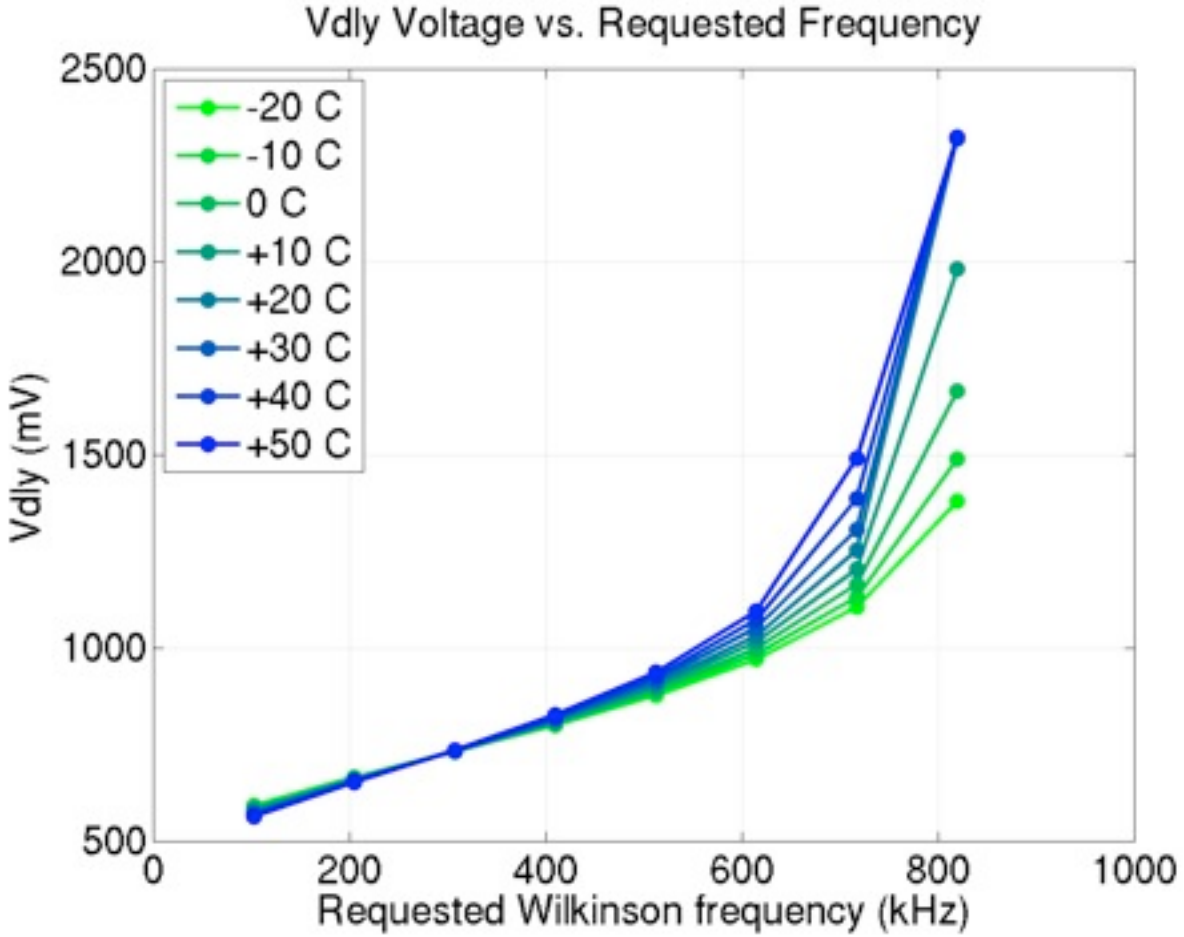
- Operating voltage ~70 V instead of ~1000 V
- Not affected by magnetic fields
- Can achieve gain (10^6) similar to PMTs
- No significant aging, compared to PMTs
- Can operate in bright light conditions, e.g. moonlight
  - Although with reduced CTA sensitivity, valuable for improving duty cycle of monitoring campaigns and for electron/positron measurement
- Compact, light, mechanically robust
- Significant after pulsing and cross talk
- Gain is sensitive to temperature and bias voltage
  - Stabilized with temperature regulation and/or bias voltage feedback
- Dark (thermal) noise is high compared to PMTs

TARGET 1 front-end module



Vdly (controls Wilkinson counter frequency) and other control voltages vary with



- Tradeoff between optimal performance at fixed temperature vs. stable performance as temperature varies
- Currently being conservative: try to get reasonable performance from -20 to +50 C
- What temperature range will we actually operate over?

Feedback loop stabilizes Wilkinson counter frequency (and transfer function) against temperature variation